BTeV Trigger and Data Acquisition System

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Fermilab

Overview

- Brief introduction to the BTeV Trigger and Data Acquisition System (DAQ)

- WBS 1.8 – Trigger Electronics & Software
  - → Project management overview
  - → Architecture overview (see Mike Wang's Beauty 2003 talk for details)
  - → Trigger R&D (results are used to determine cost and schedule)
    - segment tracker, segment matcher, hash sorter, L1 pre-prototype
  - → Comments from Temple Review 2002
  - → OpenPlan cost and schedule profiles for WBS 1.8

- WBS 1.9 – Event Readout and Controls Electronics & Software (DAQ)
  - → Project management overview
  - → Major components of the DAQ
  - → Comments from Temple Review 2002
  - → OpenPlan cost and schedule profiles for WBS 1.9

- Concluding remarks and list of talks prepared for the Breakout Session tomorrow

Introduction

1) The challenge for the BTeV trigger and data acquisition system is to analyze particle tracks and interaction vertices for every interaction that occurs in the BTeV detector (15 million/second at a luminosity of 2×10^{32}), and select interactions with *B* decays.

2) The trigger performs this task using 3 stages, referred to as Levels 1, 2 and 3:
"L1" – looks at every interaction, and rejects at least 98% of minimum bias background
"L2" – uses L1 computed results & performs a more refined analysis for data selection
"L3" – performs a complete analysis using all available data for an interaction

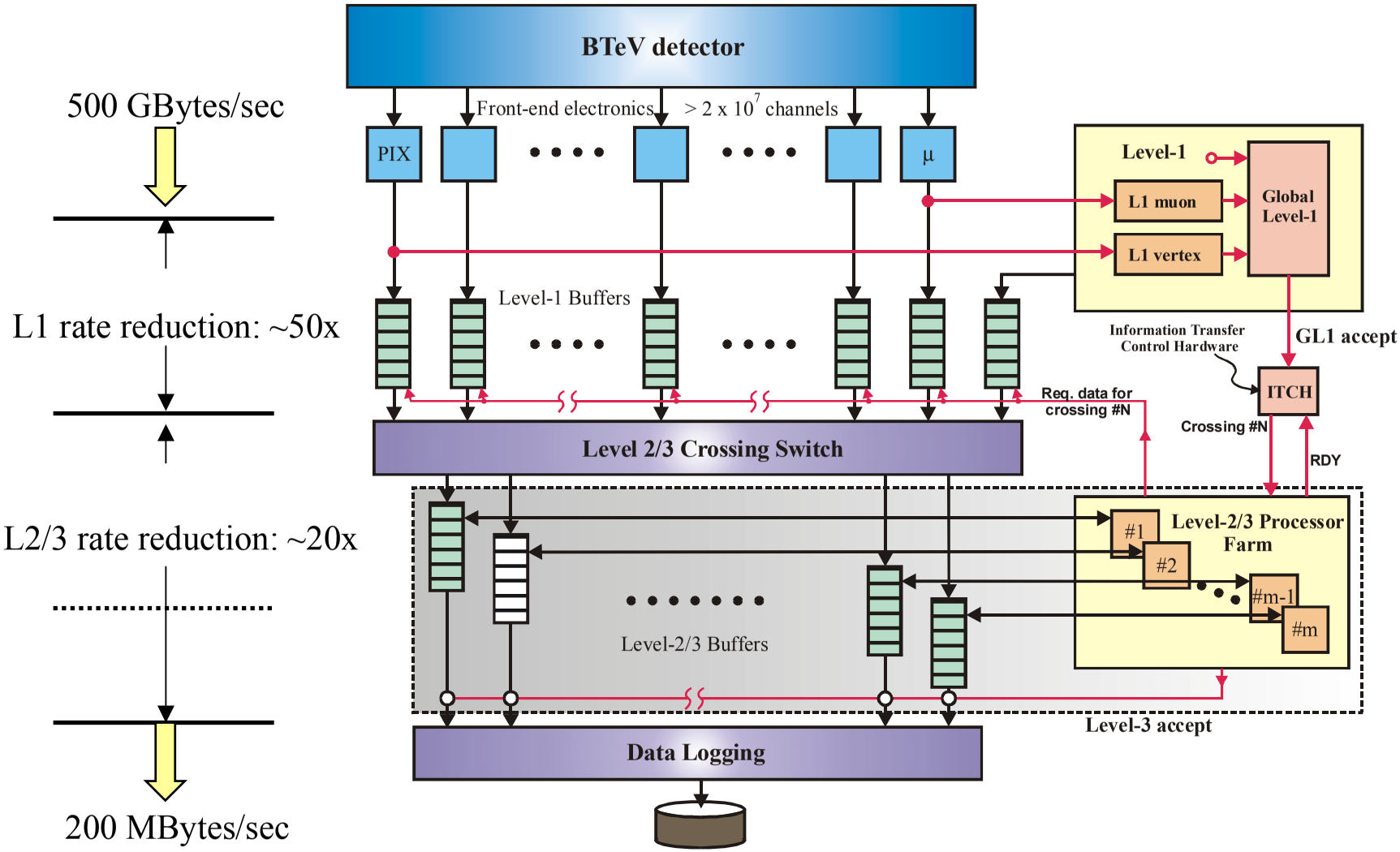
Reject > 99.9% of background. Keep > 50% of *B* events.

3) The data acquisition system saves all of the data in memory for as long as is necessary to analyze each interaction (~ 0.7 millisecond on average for L1), and moves data to processing units and archival data storage for selected interactions.

4) The key ingredients that make it possible to meet this challenge:
- BTeV pixel detector with its exceptional pattern recognition capabilities
- rapid development in technology – FPGAs, DSPs, microprocessors
- good ideas

FPGAs – field programmable gate arrays
DSPs – digital signal processors

Block Diagram of the BTeV Trigger and DAQ



BTeV Trigger

- L1 pixel trigger (FPGAs, DSPs, L1 switch)
- L1 muon trigger (same hardware as L1 pixel trigger)
- Global Level 1 trigger (same DSP hardware)
- L2/3 hardware (Linux PC farm)
- L2/3 software (similar to HEP "offline" analysis)
- RTES software (fault detection and mitigation)

Base cost: $12.0M (Material: $6.9M, Labor: $5.1M)
+ $5M grant for RTES (NSF ITR program)

BTeV Trigger Electronics & Software

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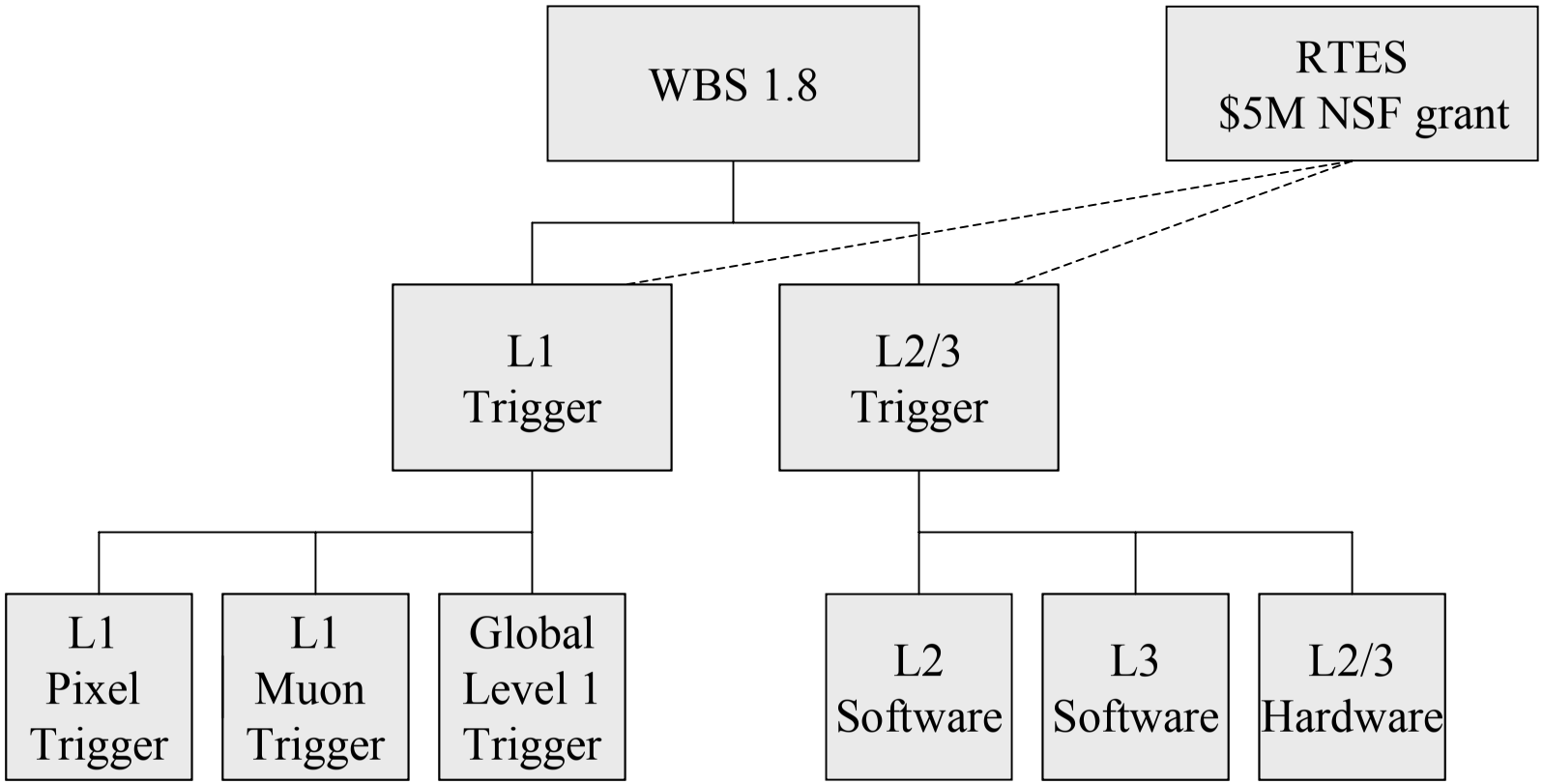

BTeV Trigger Electronics & Software

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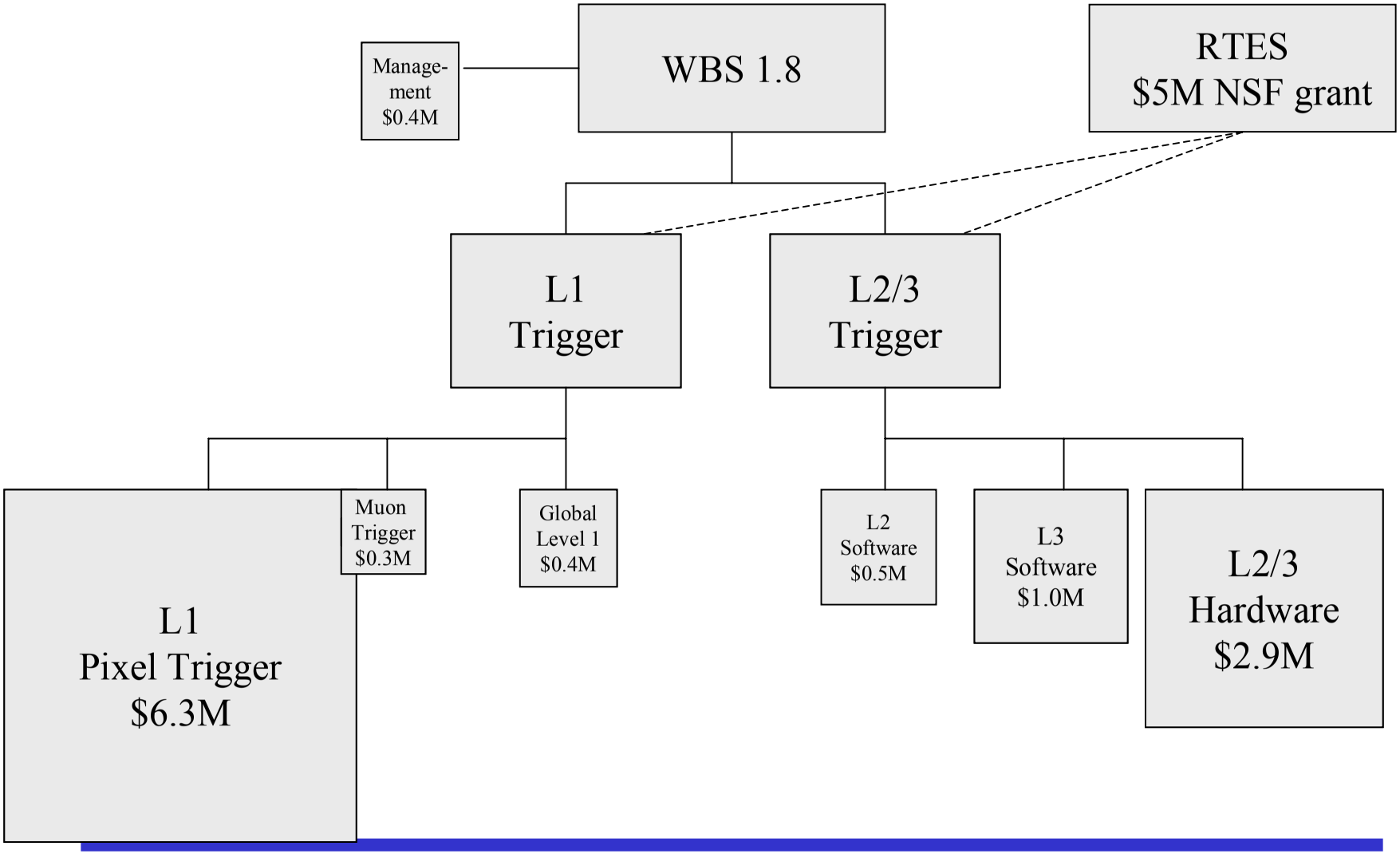
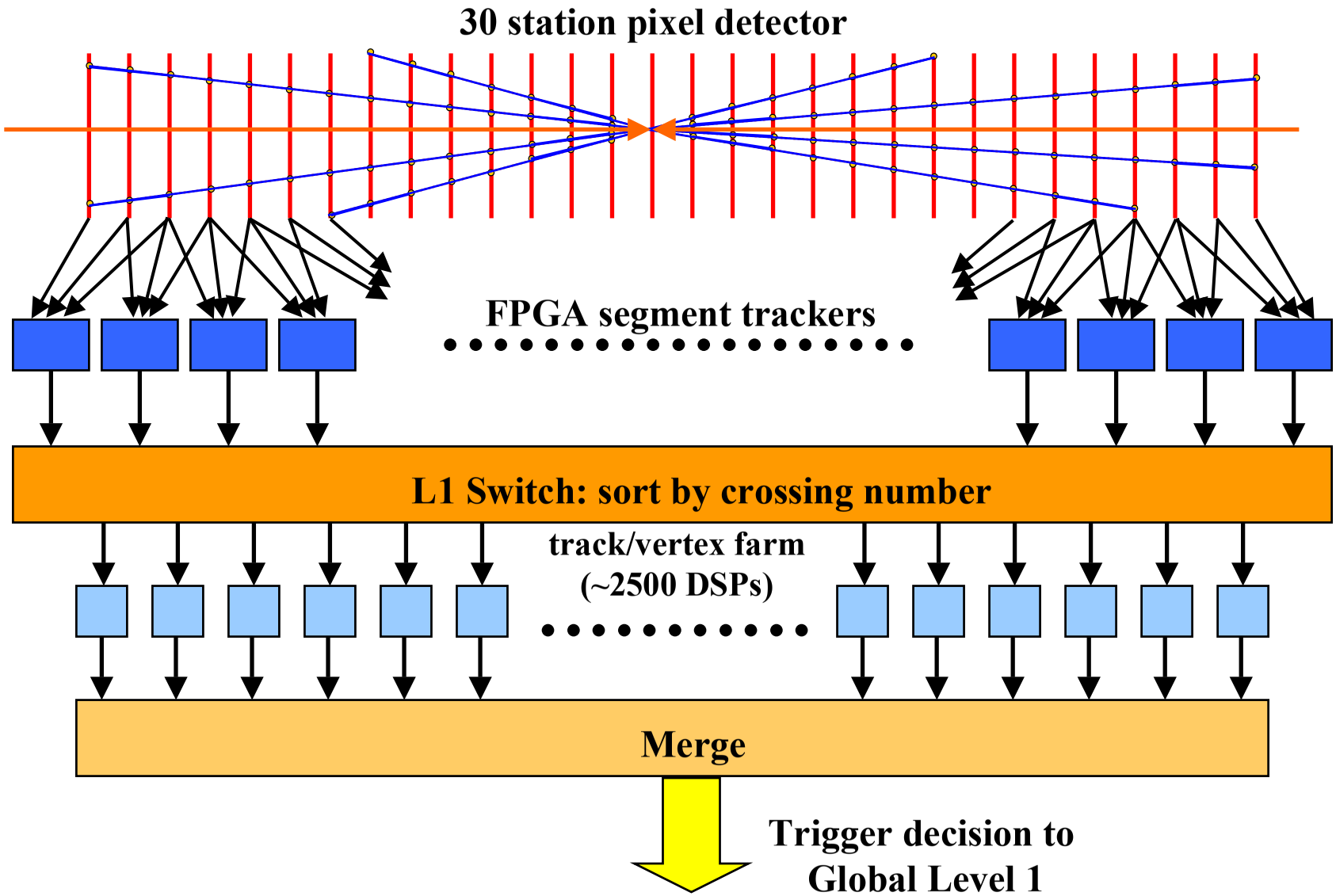
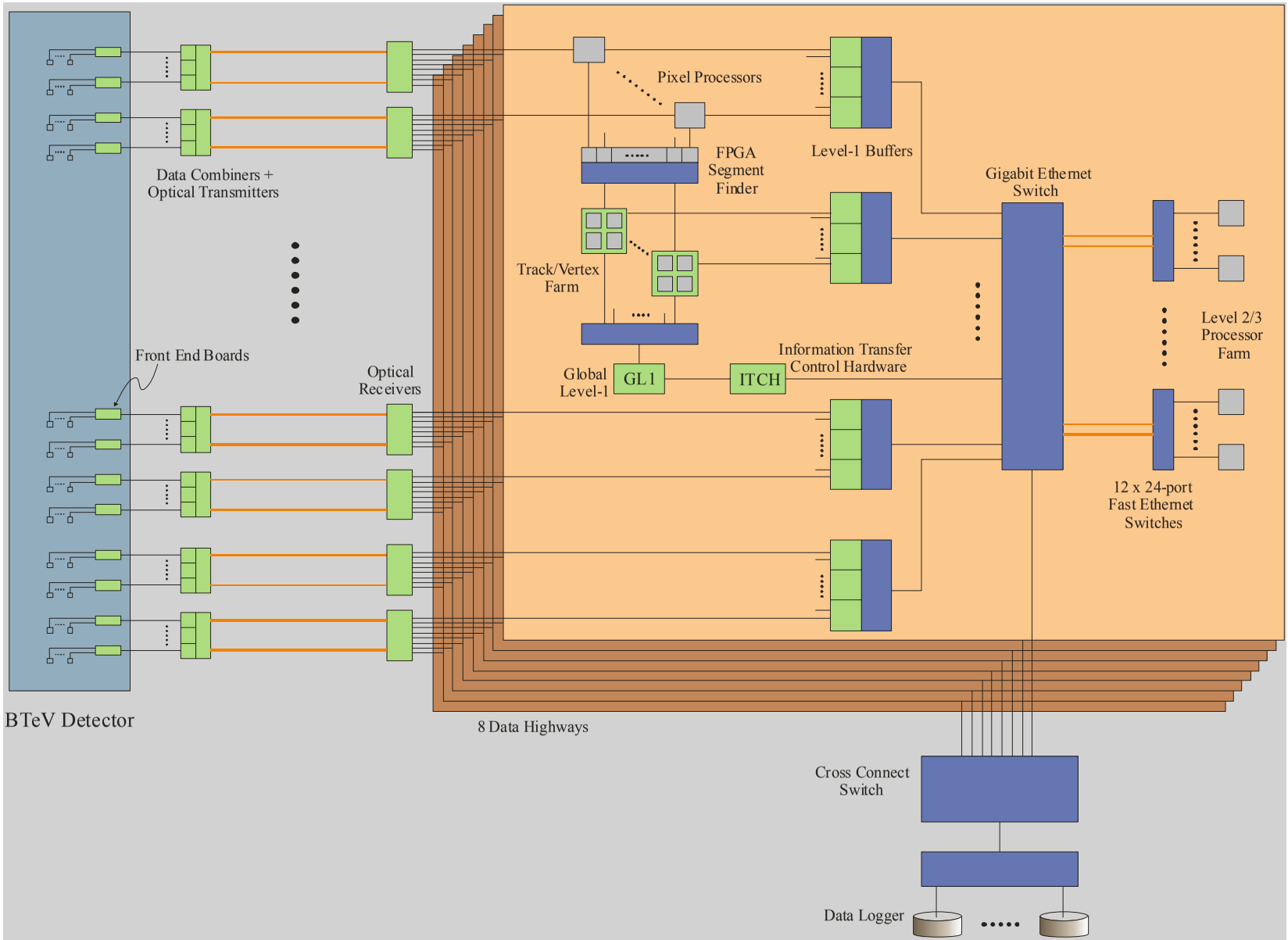


L1 pixel trigger architecture

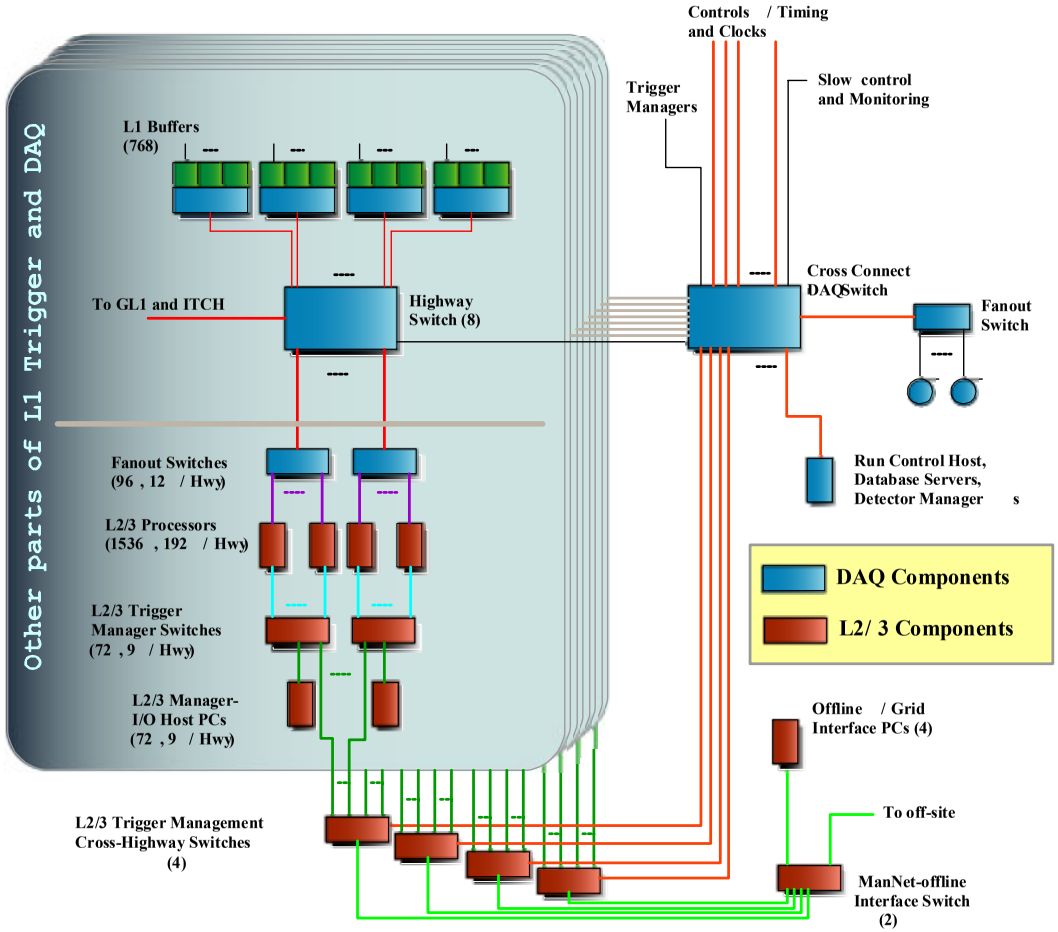


Three-level, eightfold-way trigger/DAQ architecture



L2/3 Trigger Hardware

Highway-Network View



Baseline Design

- L2/3 Processor farm consists of 1536 "12 GHz" CPUs in dual-CPU 1U rack-mount PCs
- L2/3 Trigger includes L2/3 Trigger Manager-I/O Host PCs, for database caches, worker manager/server/monitoring, and event pool cache
- L2/3 Hardware in

L2 and L3 Trigger Software

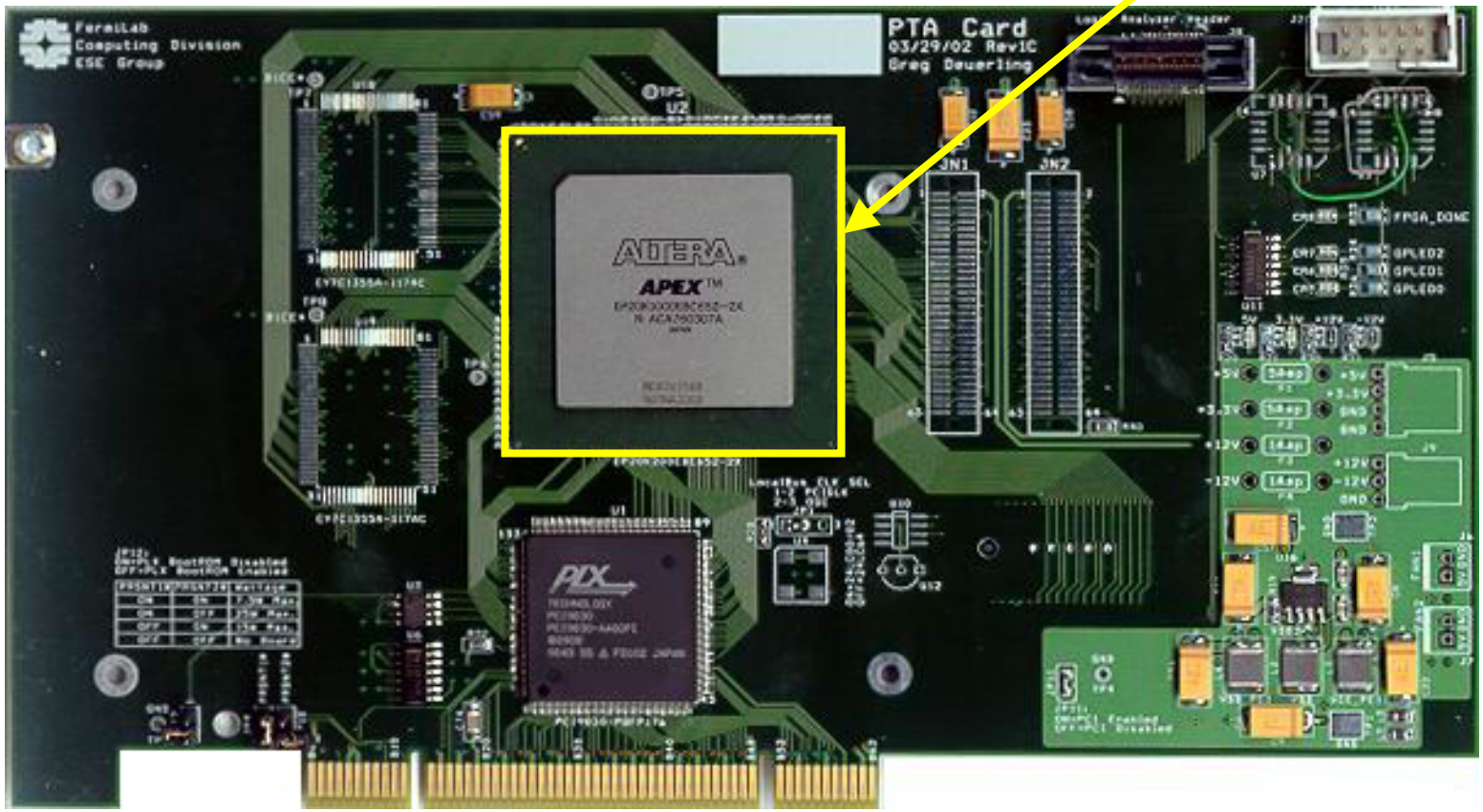
- L2 and L3 reconstruction software (tracks, photons, π^0's, Vees, particle ID, etc.)
- L2 and L3 trigger algorithms (selection criteria)
- Global L2 and Global L3 software (combinations of selection criteria and trigger lists)
- Alignment and Calibration software
- Monitoring and event display software
- Software framework utilities and interfaces to databases
- DAQ interface software (interfaces to actual DAQ hardware)
- Trigger specific system software (run control, control and monitoring, and databases)
- "L4" offline filter and fast charm/beauty monitoring software (specific selection and monitoring software needed before full L2/3 operational)

Trigger R&D (used to determine cost and schedule)

- The FPGA segment tracker algorithm (L1 pattern recognition) has been implemented on an Altera FPGA. This validates the segment-finding algorithm, and provides a basis for cost estimates (see next slide).
- Queuing simulations have been performed to address concerns raised by the June 2000 Technical Review of the BTeV trigger. Queue sizes and communication-channel bandwidths are within reasonable margins.
- A 4-DSP pre-prototype system has been built to validate the design of the L1 DSP farm, and to determine costs associated with this part of the L1 trigger.
- DSP timing studies have been performed for L1 pixel and L1 muon algorithms on aTexas Instruments C6711 floating-point DSP. This provides a basis for cost estimates.
- A hash sorter has been developed to move some DSP calculations to an FPGA that is already included in the current design. Furthermore, an FPGA segment matcher is being investigated to move additional DSP calculations to an FPGA.
- Studies of alternative processors (e.g. Pentium processors) have been performed. Results suggest that alternative processors exceed estimates presented in the BTeV Proposal and Technical Design Report (TDR) by factors of 2 or 3 in performance.

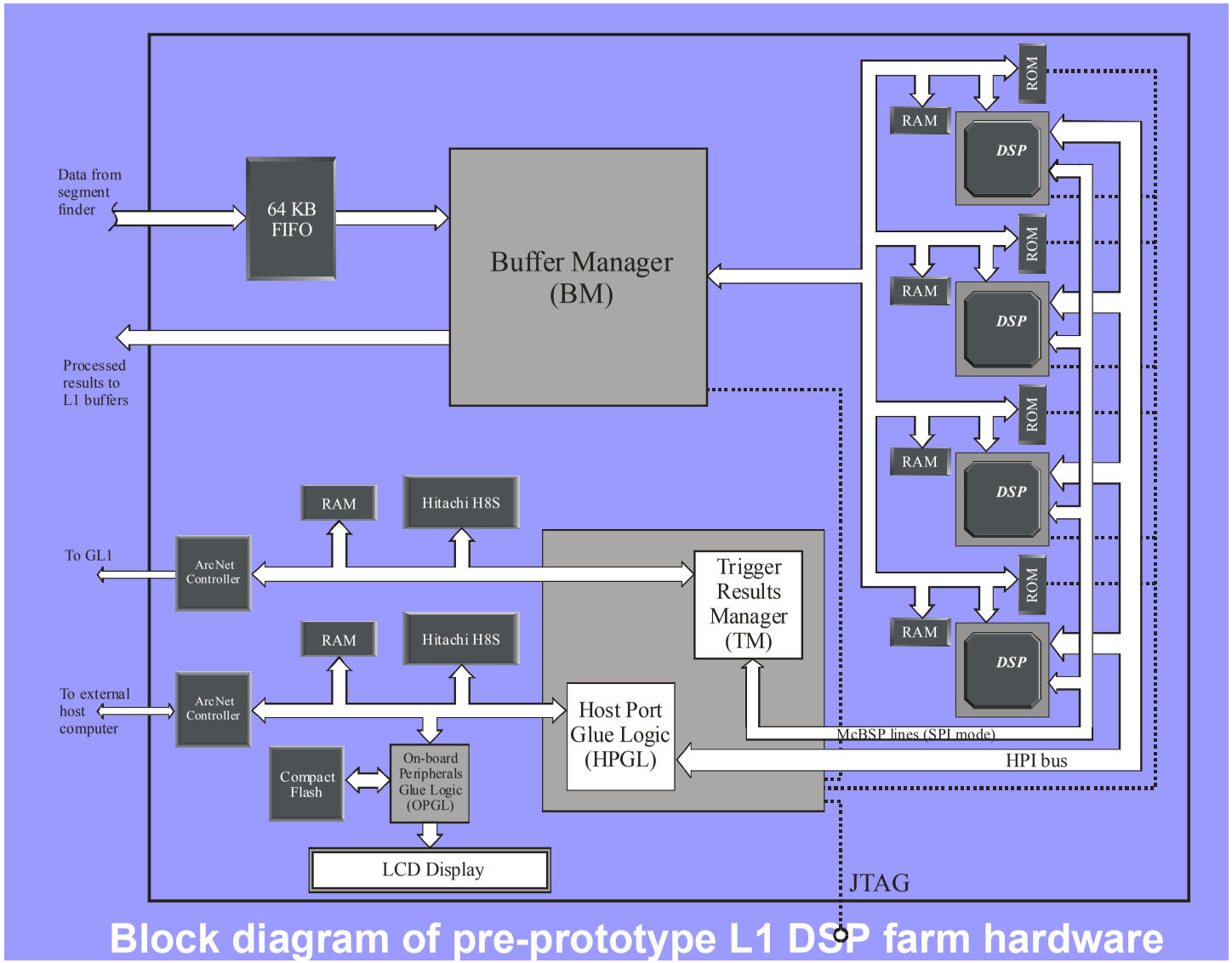
FPGA Segment Tracker R&D

Uses Altera APEX EPC20K1000 instead of EP20K200 on regular PTA



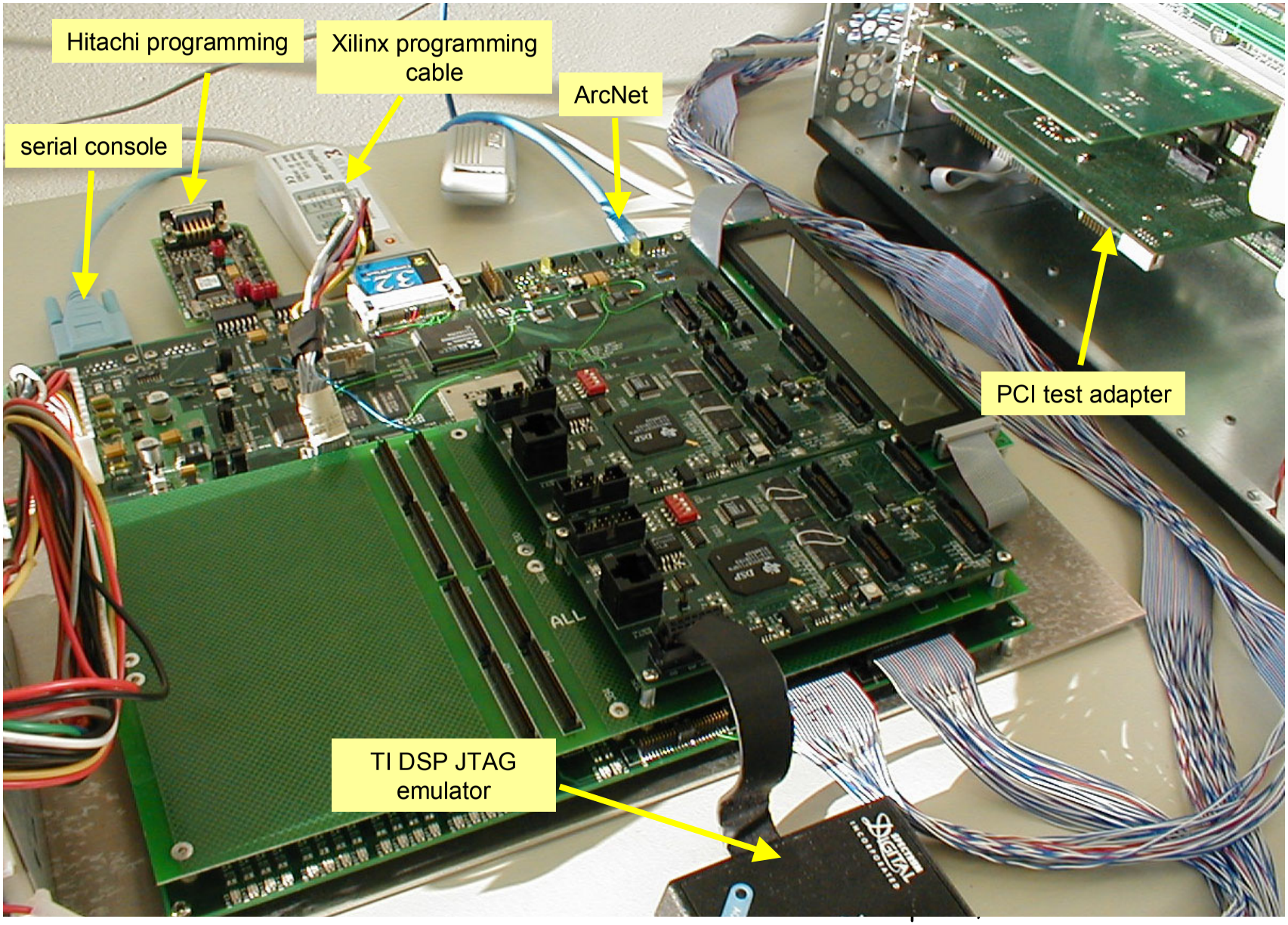
Modified version of PCI Test Adapter (PTA) card developed at Fermilab for testing hardware implementation of FPGA segment tracker (a.k.a. “Super PTA”)

L1 DSP Farm R&D



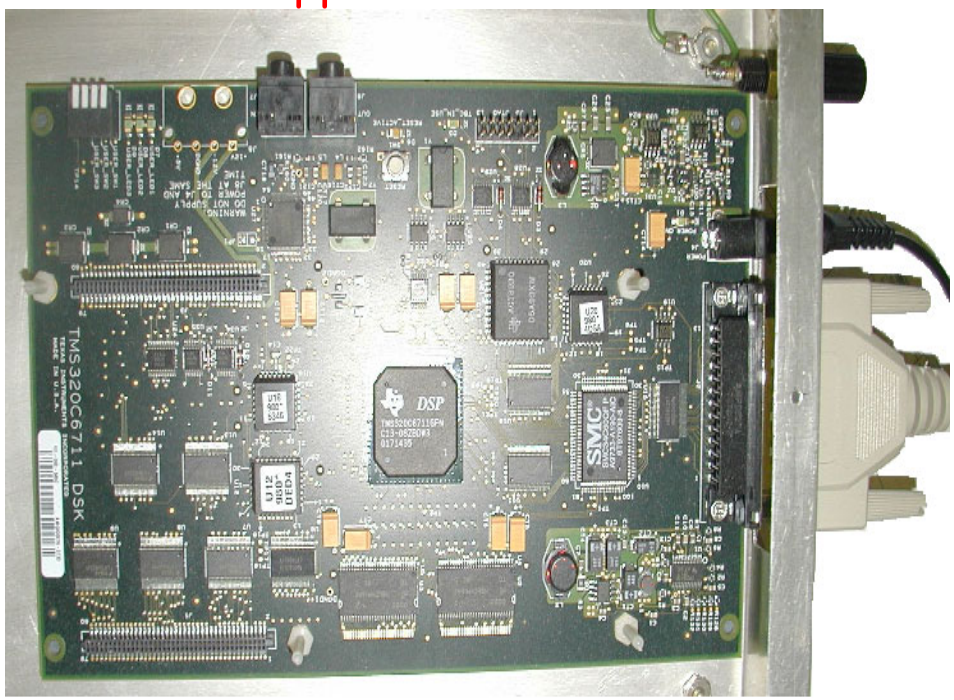
Block diagram of pre-prototype L1 DSP farm hardware

L1 Pre-prototype Test Stand



Size & Speed of L1 Muon Trigger Code

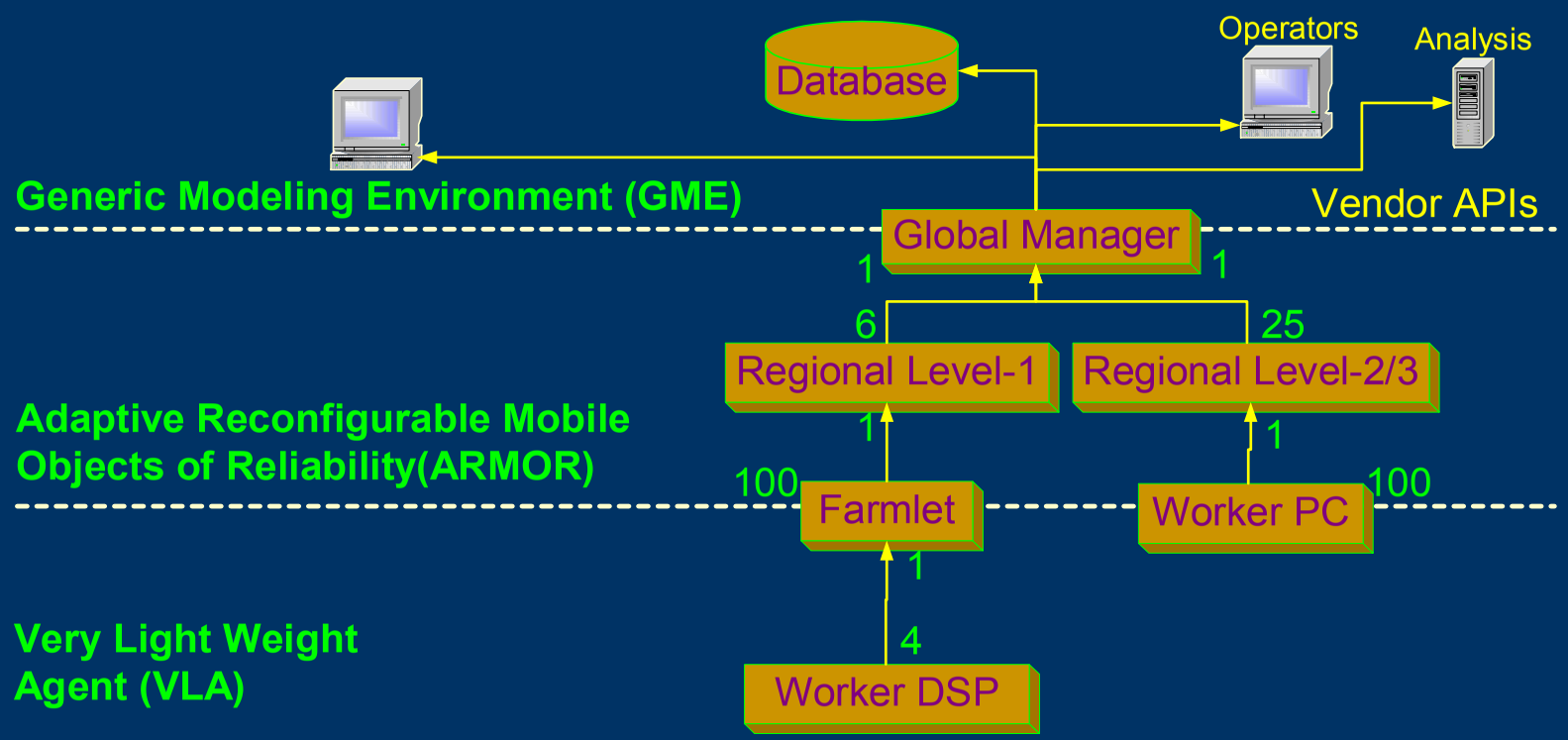
- Work done by UIUC grad student John Cassel (also on RTES):
  - Implemented "clock-cycle" counting technique for timing tests.
  - Optimized muon trigger code (used for simulations) for DSP
  - Achieved DSP results for efficiency & rejection that satisfy requirements
  - The results support the cost estimates for the L1 muon trigger



TMS320C6711

Real Time Embedded Systems (RTES) R&D

- RTES: NSF ITR (Information Technology Research) funded project
- Collaboration of computer scientists, physicists & engineers from: University of Illinois, Pittsburgh, Syracuse, Vanderbilt & Fermilab
- Working to address the reliability of large-scale clusters with real time constraints
- BTeV trigger provides a testbed for RTES on which to conduct their research and apply their solutions



RTES demonstration for Super Computing 2003

- RTES university groups & Fermilab are working together to create a system (hardware and software) demonstrating their technology in a BTeV L1 trigger-like setting
- This is a demonstration project that has a deadline, and it is a system that will be reviewed
- This demonstration project is helping RTES groups develop an understanding of the processing that is done by the BTeV trigger
- They are developing code and rules that handle some of the problems we expect to encounter
- The system contains initial prototypes of the deliverables: GME models, ARMORs, and VLAs

Temple Review 2002

Trigger Electronics and Software (WBS 1.8)

- the trigger did very well in the Temple Review
- no change in base cost or contingency
- findings and comments were generally positive:

> "The proponents are to be congratulated for several major advances that have reduced the technical risk of the trigger system. Notable among these advances are the use of C-code compilers for the generation of DSP Level-1 trigger code and the movement toward commercial switch hardware."

OpenPlan Total Construction Cost Profile

BTeV - WBS 1.8 TRIGGER
Total Construction Cost Profile ($K) by Institution & Fiscal Year
Fermilab Labor: Salary, OPTO, Vacation, Fringe & Overhead
Non-Fermilab Labor: Salary, Benefits & Overhead
No Contingency, No Escalation, No Full material Procurement 'Burdening'

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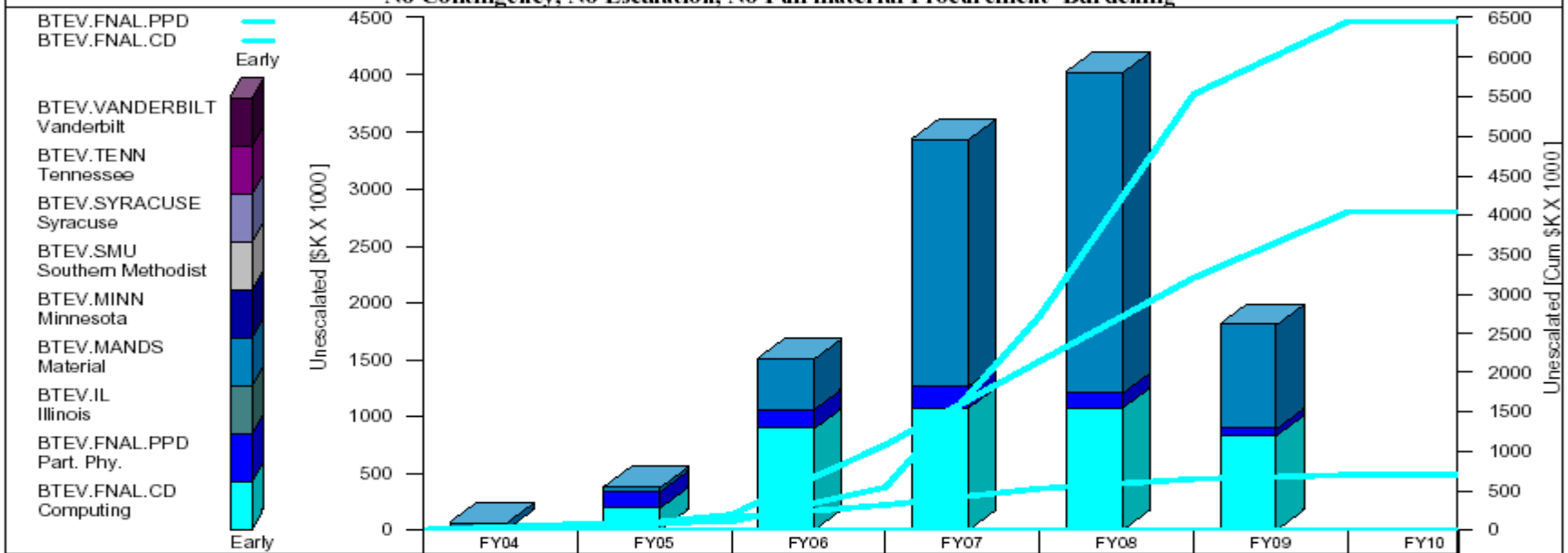
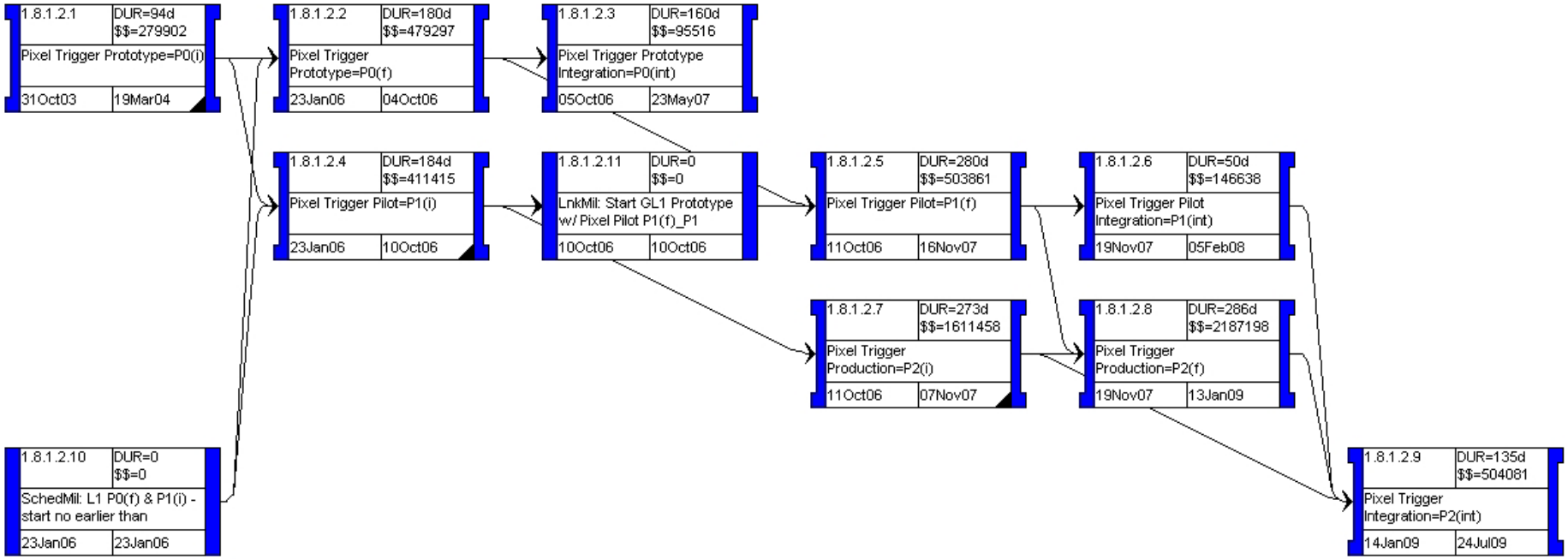
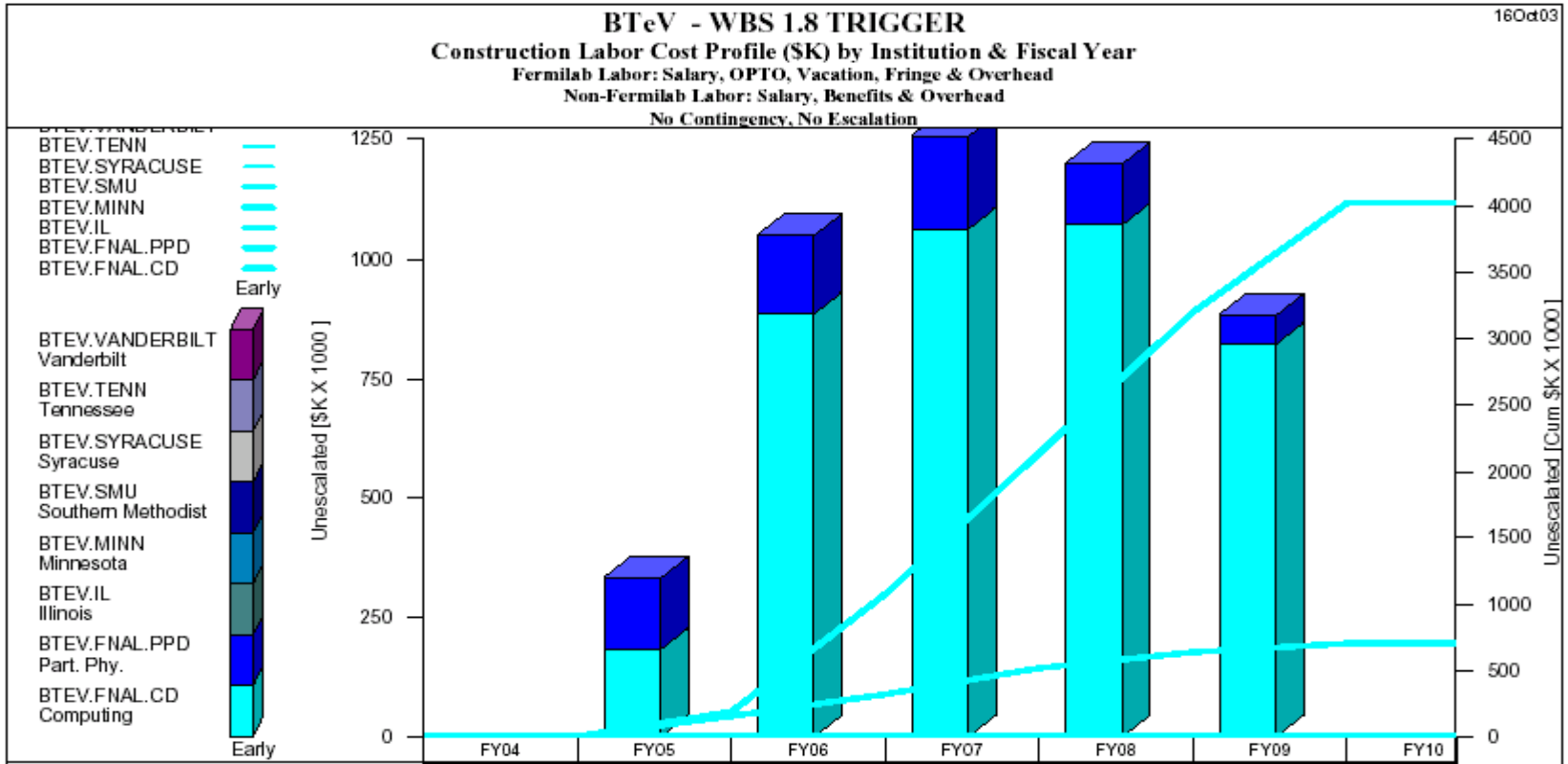


	FY04	FY05	FY06	FY07	FY08	FY09	FY10
BTEV.FNAL.CD : Computing	0	182	883	1060	1071	819	
BTEV.FNAL.PPD : Part. Phy.	0	149	164	193	126	60	
BTEV.IL : Illinois	0	0	0	0	0	0	
BTEV.MANDS : Material	55	34	446	2169	2814	915	
BTEV.MINN : Minnesota	0	0	0	0	0	0	
BTEV.SMU : Southern Methodist	0	0	0	0	0	0	
BTEV.SYRACUSE : Syracuse	0	0	0	0	0	0	
BTEV.TENN : Tennessee	0	0	0	0	0	0	
BTEV.VANDERBILT : Vanderbilt	0	0	0	0	0	0	
BTEV.FNAL.CD : Computing [Cum]	0	182	1065	2125	3196	4015	
BTEV.FNAL.PPD : Part. Phy. [Cum]	0	149	313	506	631	692	
BTEV.IL : Illinois [Cum]	0	0	0	0	0	0	
BTEV.MANDS : Material [Cum]	55	89	535	2704	5518	6433	
BTEV.MINN : Minnesota [Cum]	0	0	0	0	0	0	
BTEV.SMU : Southern Methodist [Cum]	0	0	0	0	0	0	
BTEV.SYRACUSE : Syracuse [Cum]	0	0	0	0	0	0	
BTEV.TENN : Tennessee [Cum]	0	0	0	0	0	0	
BTEV.VANDERBILT : Vanderbilt [Cum]	0	0	0	0	0	0	

L1 Pixel Trigger OpenPlan View

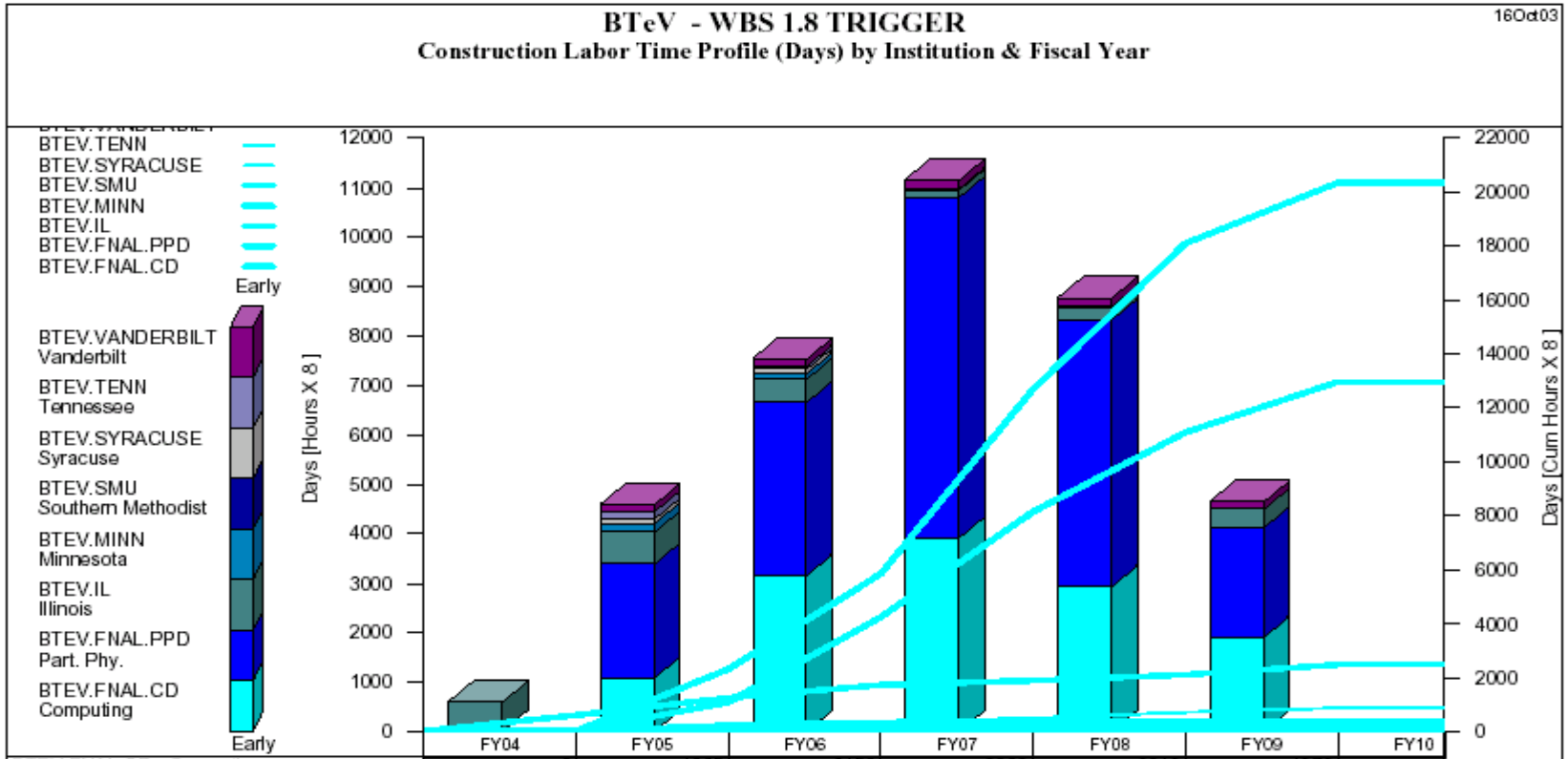


OpenPlan Labor Cost Profile



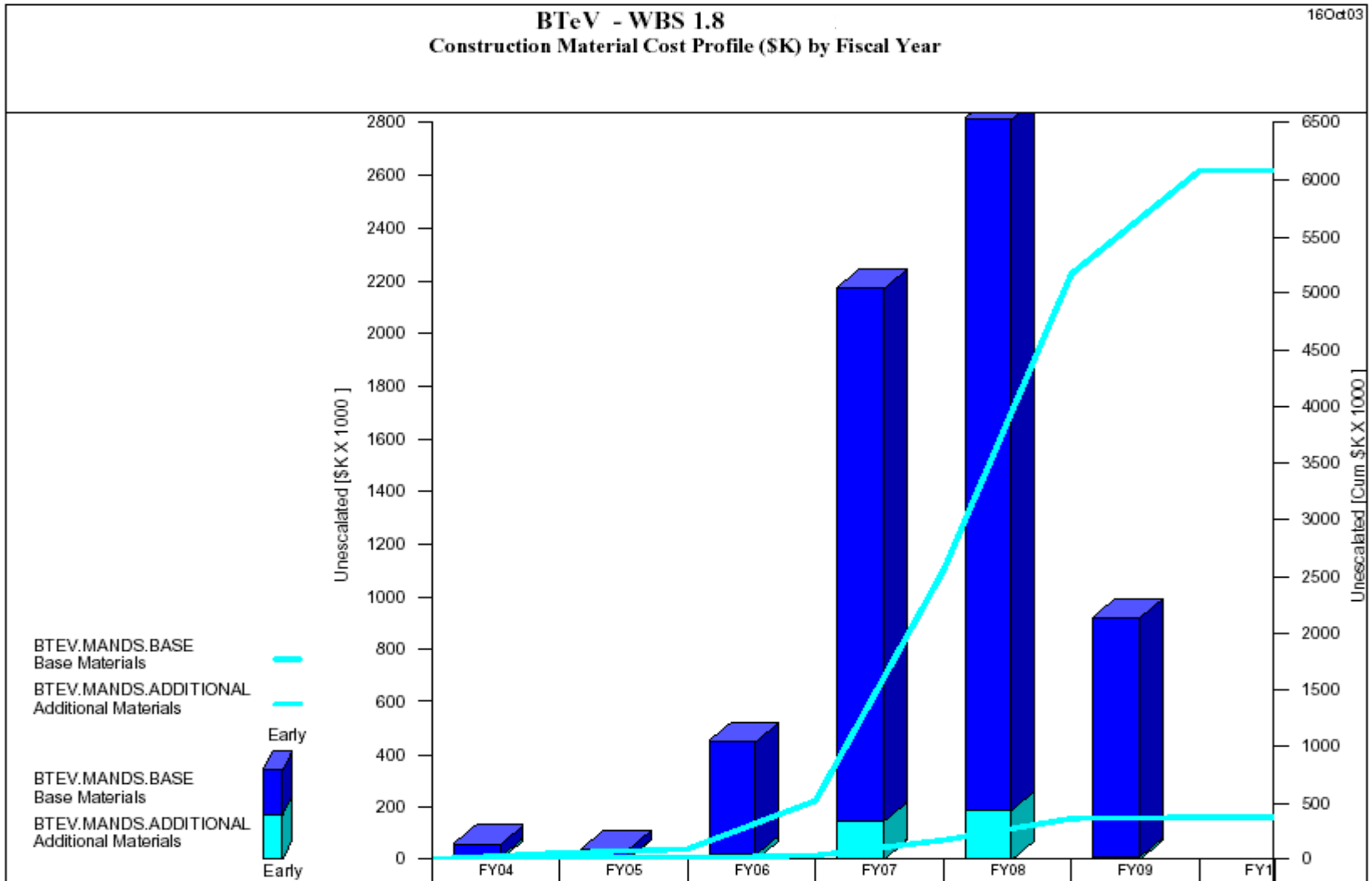
	FY04	FY05	FY06	FY07	FY08	FY09	FY10
BTEV.FNAL.CD : Computing	0	182	883	1060	1071	819	
BTEV.FNAL.PPD : Part. Phy.	0	149	164	193	126	60	
BTEV.IL : Illinois	0	0	0	0	0	0	
BTEV.MINN : Minnesota	0	0	0	0	0	0	
BTEV.SMU : Southern Methodist	0	0	0	0	0	0	
BTEV.SYRACUSE : Syracuse	0	0	0	0	0	0	
BTEV.TENN : Tennessee	0	0	0	0	0	0	
BTEV.VANDERBILT : Vanderbilt	0	0	0	0	0	0	
BTEV.FNAL.CD : Computing [Cum]	0	182	1065	2125	3196	4015	
BTEV.FNAL.PPD : Part. Phy. [Cum]	0	149	313	506	631	692	
BTEV.IL : Illinois [Cum]	0	0	0	0	0	0	
BTEV.MINN : Minnesota [Cum]	0	0	0	0	0	0	
BTEV.SMU : Southern Methodist [Cum]	0	0	0	0	0	0	
BTEV.SYRACUSE : Syracuse [Cum]	0	0	0	0	0	0	
BTEV.TENN : Tennessee [Cum]	0	0	0	0	0	0	
BTEV.VANDERBILT : Vanderbilt [Cum]	0	0	0	0	0	0	

OpenPlan Labor Time Profile



	FY04	FY05	FY06	FY07	FY08	FY09	FY10
BTEV.FNAL.CD : Computing	0	1065	3150	3903	2918	1878	
BTEV.FNAL.PPD : Part. Phy.	0	2302	3493	6878	5389	2228	
BTEV.IL : Illinois	564	638	470	166	246	367	
BTEV.MINN : Minnesota	0	182	127	24	9	8	
BTEV.SMU : Southern Methodist	0	0	0	0	0	0	
BTEV.SYRACUSE : Syracuse	0	96	62	4	0	0	
BTEV.TENN : Tennessee	0	132	78	0	0	0	
BTEV.VANDERBILT : Vanderbilt	0	152	151	175	184	145	
BTEV.FNAL.CD : Computing [Cum]	0	1065	4216	8119	11036	12914	1
BTEV.FNAL.PPD : Part. Phy. [Cum]	0	2302	5795	12673	18062	20290	2
BTEV.IL : Illinois [Cum]	564	1202	1672	1838	2083	2450	
BTEV.MINN : Minnesota [Cum]	0	182	309	333	342	350	
BTEV.SMU : Southern Methodist [Cum]	0	0	0	0	0	0	
BTEV.SYRACUSE : Syracuse [Cum]	0	96	158	163	163	163	
BTEV.TENN : Tennessee [Cum]	0	132	210	210	210	210	
BTEV.VANDERBILT : Vanderbilt [Cum]	0	152	303	478	663	808	

OpenPlan Material Cost Profile



	FY04	FY05	FY06	FY07	FY08	FY09	FY1
BTEV.MANDS.ADDITIONAL : Additional Materials	7	3	16	141	188	7	
BTEV.MANDS.BASE : Base Materials	48	31	430	2028	2626	907	
BTEV.MANDS.ADDITIONAL : Additional Materials [Cu	7	10	25	167	355	362	
BTEV.MANDS.BASE : Base Materials [Cum]	48	80	510	2537	5163	6070	

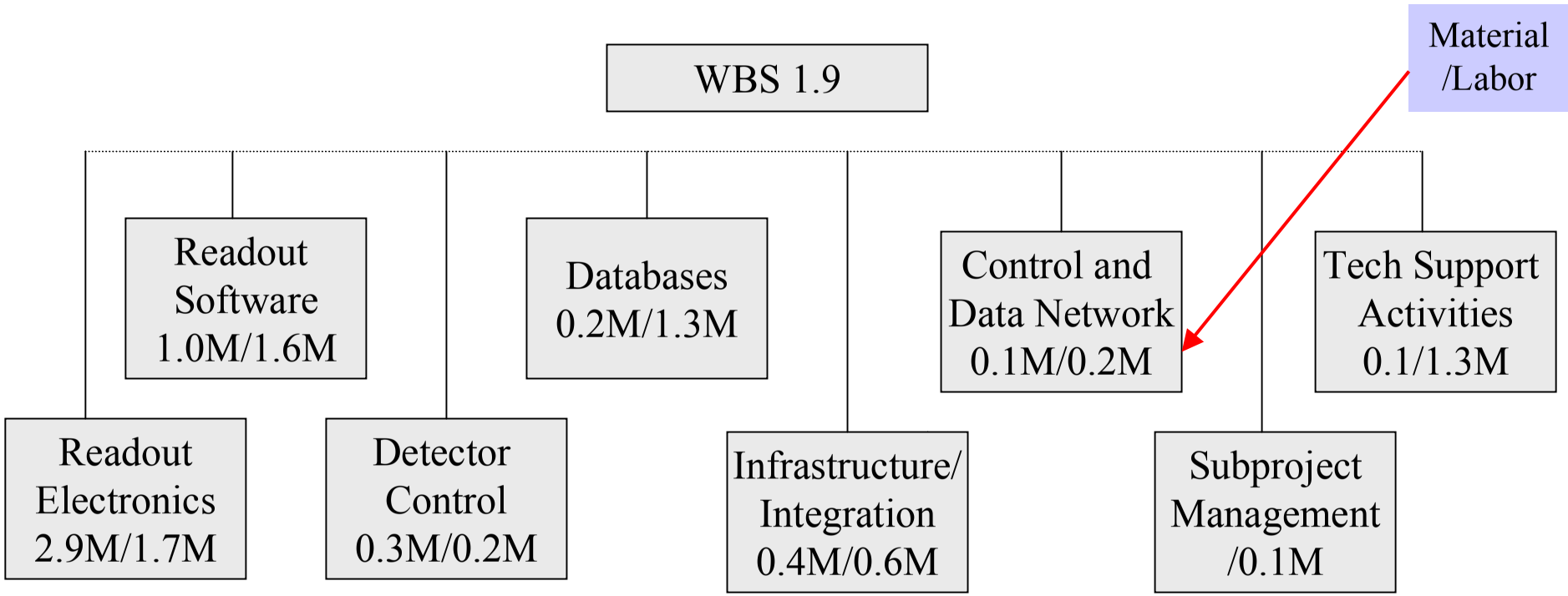
BTeV Readout and Controls (DAQ)

- Readout electronics
- Data acquisition software
- Detector control system
- Databases
- Control & data network
- Technical Support

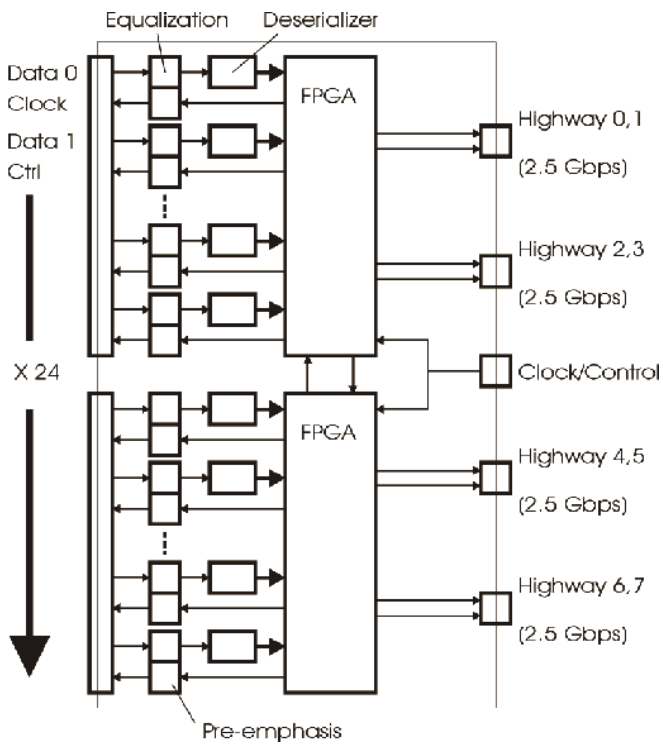
Base cost: $12.1M (Material: $5.1M, Labor: $7.0M)

WBS 1.9 – Readout, Controls Electronics & Software

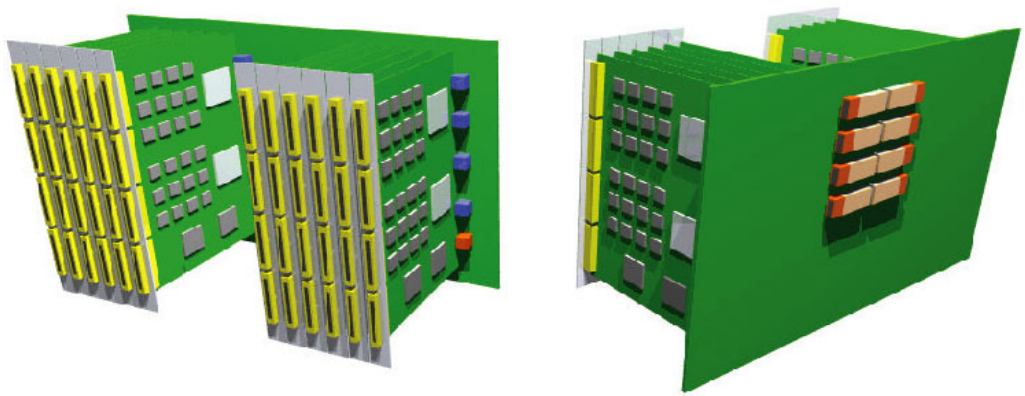
Base cost: $12.1M (Material: $5.0M, Labor: $7.0M)



Data Combiner Boards (DCBs)

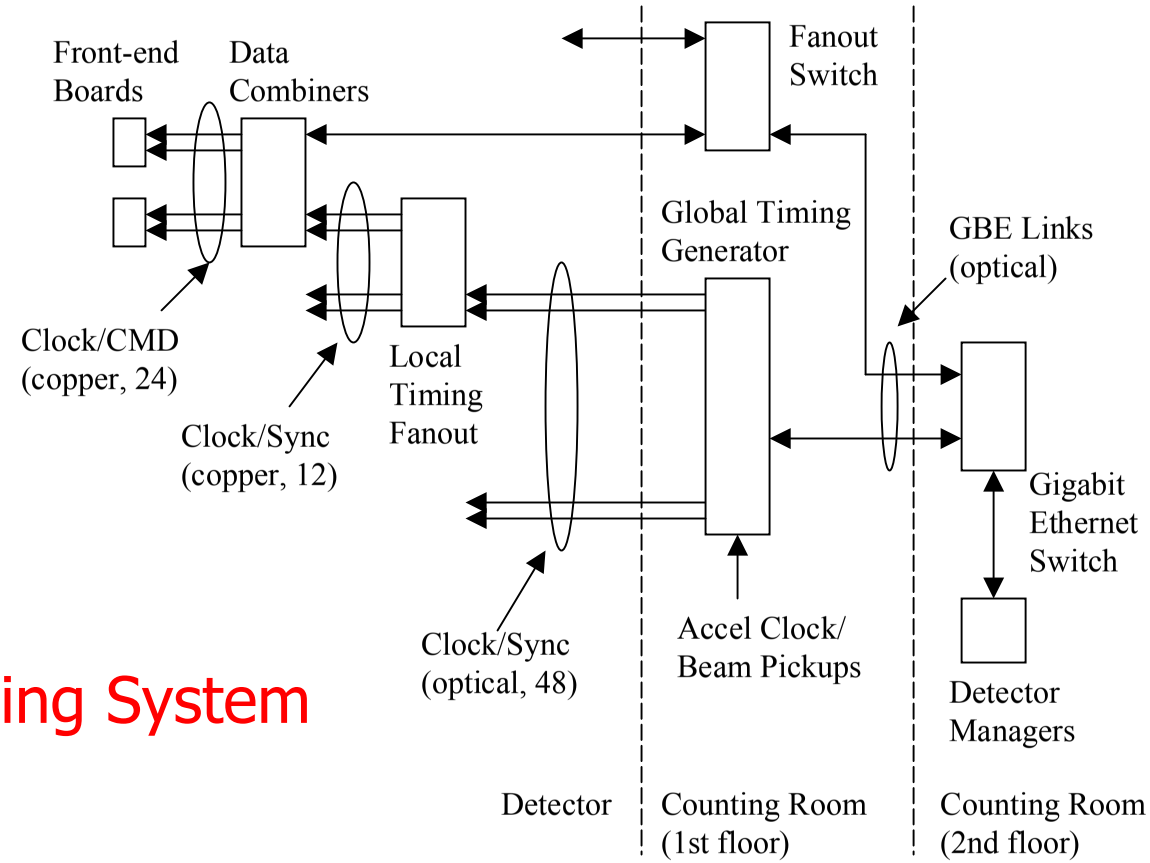


Data Combiner



Input receiver/multiplexer for all (non-triggered) detector front-end boards.

Timing System



Timing System

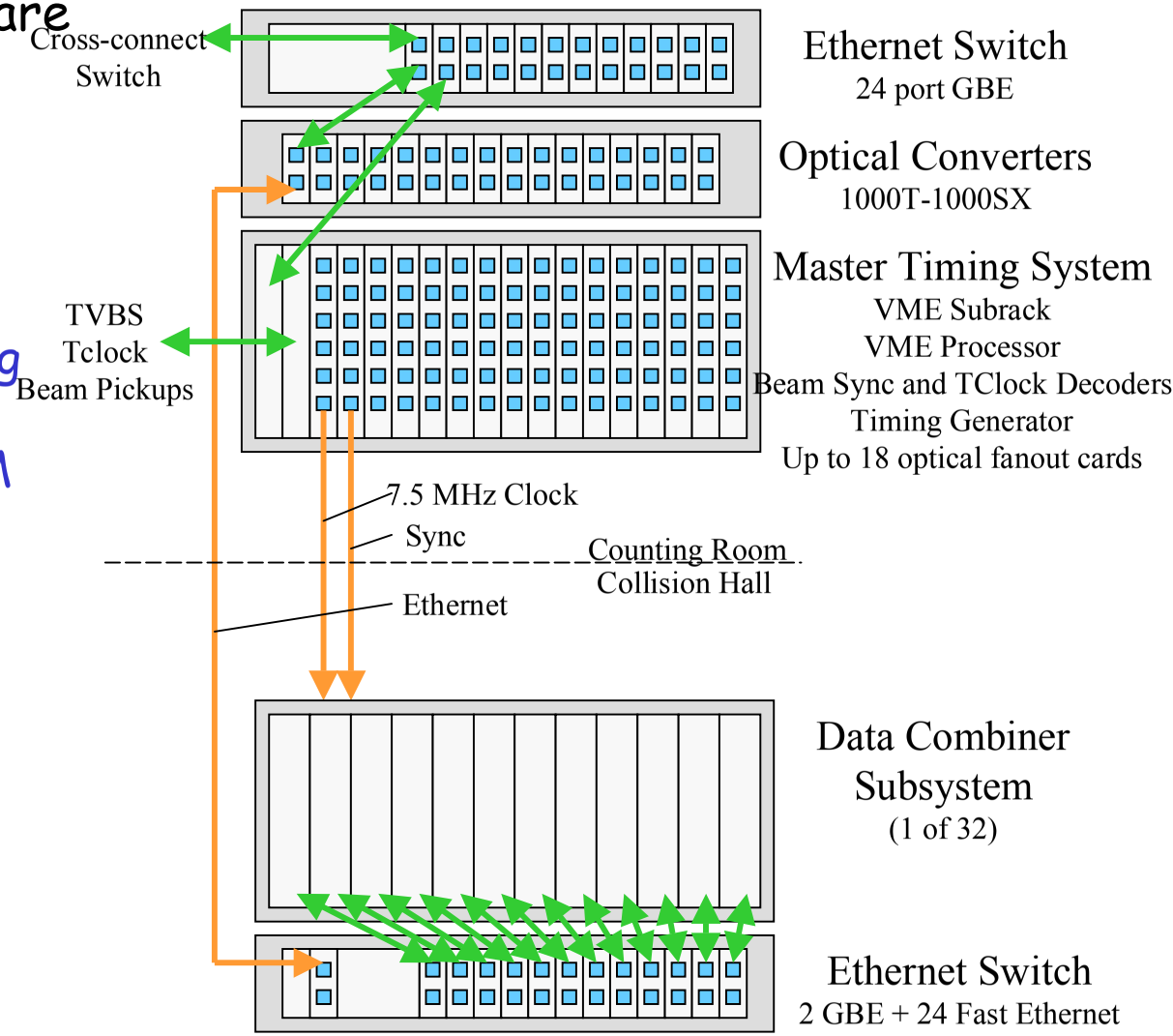
Fast control and timing distribution network for precise system synchronization.

Timing System

- Generate and distribute signals synchronized with the accelerator clock
- 1 ns or better precision resolution/jitter
- 7.5 MHz clock and sync signals are delivered to each DCB subsystem.
- Control message (start/stop/calibrate) are sent asynchronously over Ethernet. Commands are activated at a predifined (bunch crossing) clock signal
- DCB modules perform fine-grain timing and clock phase adjustments (for each front-end link)
- Static timing information – e.g. bunch fill patterns – will be stored in the DCBs.
- Since the data is send from the detector to the DCBs on every crossing no fast trigger signal or other external timing information is required.

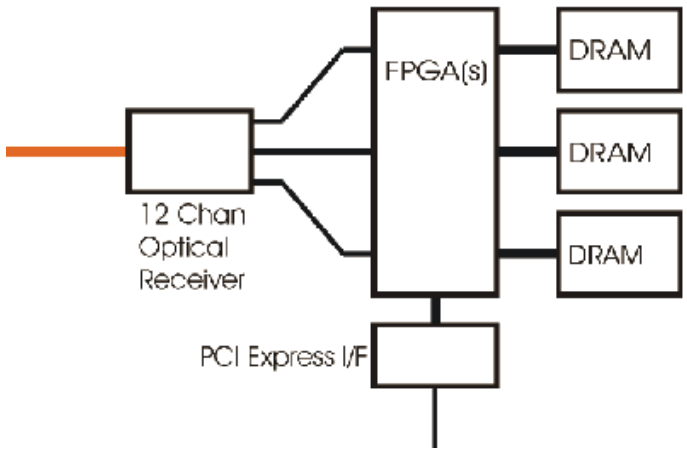
Timing System Implementation

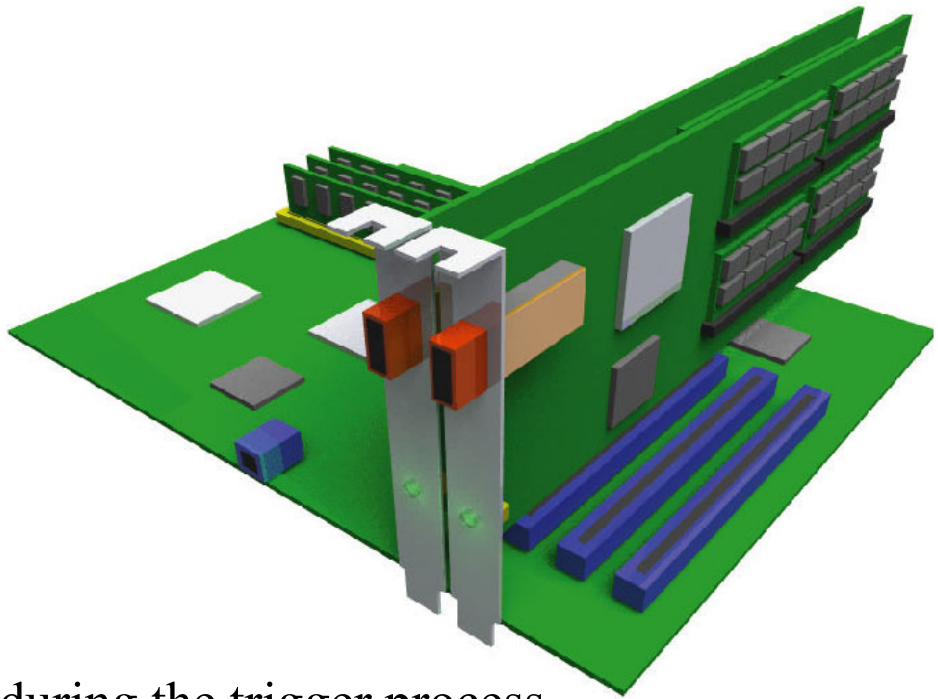
- Use commercial hardware
  - VME (CPU, crate)
  - Ethernet switches
  - Optical converters
- Use existing hardware
  - Clock decoders, timing generators developed for the Tevatron BPM project.
- Optical fan-out cards are new but simple



Level 1 Buffer

Update with new L1B prototype design



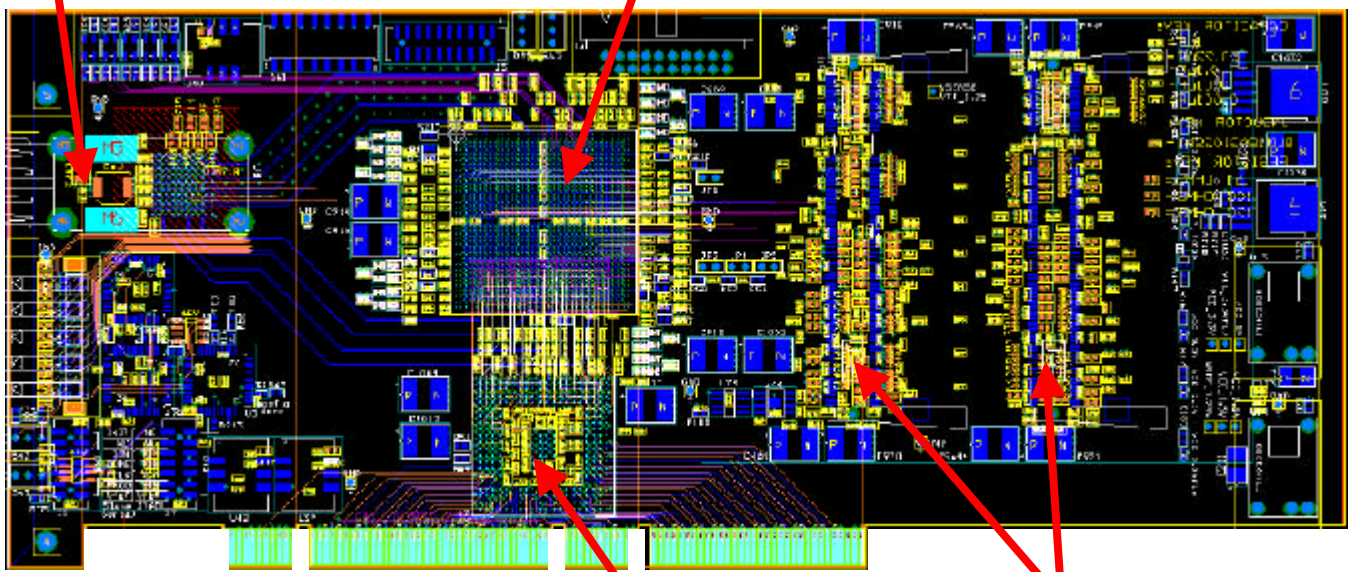


Large capacity buffers to hold data during the trigger process.

L1 Buffer Prototype

Optical Receiver (12 channels X 2.5 Gbps)

FPGA (deserializers, memory controller)



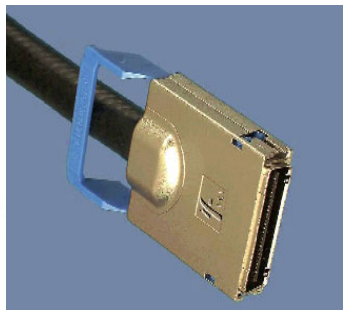
PCI Interface

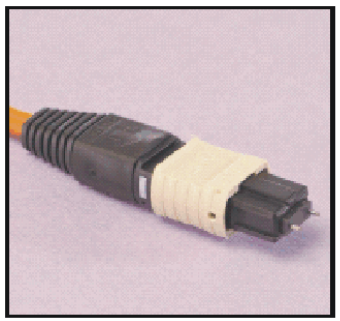
DRAM (512 MB X 2, DDR SODIMM)

- In layout, expect first boards in a month
- Standard optical interface
- Buffer memory architecture
- PCI Interface (BTeV will use a newer generation, maybe PCI-Express)

Data Links

UPDATE REQUIRED: add results from performance measurements, mention risk factor if not cat5/6 cables, contingency





Front-end to Data Combiners
- 600 Mbps copper

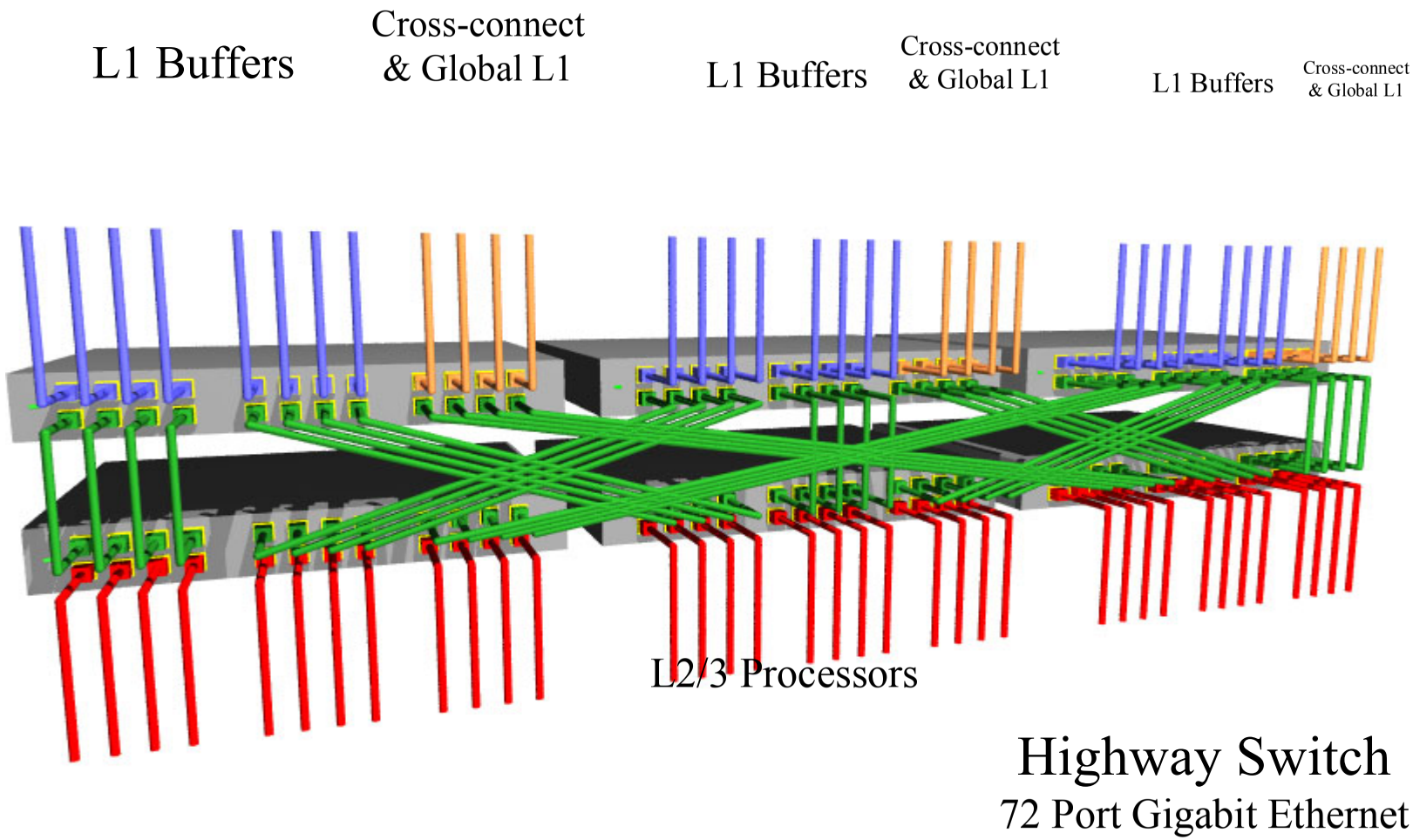
Data Combiners to L1 buffers & L1 Trigger
- 2.5 Gbps optical

L1 Trigger to L1 Buffers
- 2.5 Gbps copper

Network
- 1 Gbps (CAT6) copper

(all point-to-point serial)

Highway Switch (for a single data highway)



Other Major Components of WBS 1.9

- Configuration Subsystem - software to download, initialize and partition all system components
- Run Control Subsystem - software to control and monitor the operation and overall dataflow of the system
- Detector Control - "slow" control network to set and monitor all system environmental parameters
- Databases - store and access operating parameters, maintain a time history of all system variables, and store and access parameters necessary for trigger algorithms
- Infrastructure - counting and control room infrastructure

Temple Review 2003 WBS 1.9

- Recommendation 1: Develop a DCB prototype
  - The development of a DCB prototype will begin in Spring 2004. Since the last review, we have begun merging the DCB design for the pixel/silicon detectors with the DCB design used by other sub-detectors. Concerns that the development of the DCB prototype had to be delayed due to the DAQ funding profile have been addressed and initial support for this project will come from the pixel detector sub-project.
- Recommendation 2: Choose a clock distribution scheme and prototype the corresponding hardware. Investigate interactions with the various trigger and DAQ components
  - Our work with the Tevatron beam position monitor system allowed us to gain experience with the accelerator timing system. This led to some simplification of the BTeV timing system, as it appears likely that we will be able to re-use in BTeV some of the components developed for the BPM system. Details of the new design will be presented in the breakout sessions.

Temple Review 2003 WBS 1.9 cont'd

- Recommendation 3: Evaluate the radiation levels in the proposed DCB locations and their impact on DCB performance. Determine DCB location and verify adequate performance of the cables to the front-ends
  - Total radiation dose received by the DCB modules is not a major concern, since radiation levels at the default locations around the detector are less than 0.5KRad/yr (most integrated circuits can handle 20KRad or more). We are, however, concerned about single event upset, and we plan to implement some logic redundancy as well as continuously scrub (reload) the DCB FPGAs.
  - The performance of the data links (copper between detector and DCBs, optical between DCBs and L1 buffers) was studied several years ago. With a HP G-Link based system we obtained bit failure rates at the 10-15 level – sufficiently low for BTeV. We are planning to repeat these tests in the next months with the L1B prototype board which uses the same optical interface we intend to use for BTeV. For the links between the front-end electronics and the DCBs we will use shielded CAT 6 cables. Cat 5/6 cabling is currently used in StarGen interconnects at similar speeds and distances. The performance of these cables needs to be verified however. We listed this as a risk item and also assigned a 100% contingency to the front-end cable costs.

Trigger/DAQ Summary

- Our basic designs for both the trigger and DAQ have been stable since the BTeV Proposal (May 2000).
- The DAQ design is based on commercial networking equipment, which eliminates concerns about building a custom switch.
- The trigger system has a design that can accommodate new ideas, changes in running conditions, and new technology. The design includes FPGAs, DSPs, and PCs. We exploit the strengths of each type of hardware, and we can change our implementation as we learn more about running conditions and physics goals.
- For example: we have been studying two new ideas (hash sorter & segment matcher) that promise to improve the L1 trigger design by moving DSP calculations to FPGAs that are already included in the design.
- Another example: we are considering alternatives to DSPs (such as Pentium processors) that could provide higher performance at Level 1 for lower cost.

Concluding Remarks

More details of the BTeV Trigger (WBS 1.8) and DAQ (WBS 1.9) will be available for the breakout sessions.

WBS 1.8:

- BTeV trigger – Mike Wang (talk presented last week at Beauty 2003)
- L1 pixel trigger – Vince Pavlicek
- L1 muon trigger algorithm – Mats Selen
- L1 muon trigger – Mike Haney
- Global Level 1 – Vince Pavlicek
- L2/3 hardware – Harry Cheung
- L2/3 software – Paul Lebrun
- RTES – Jim Kowalkowski

WBS 1.9:

- Overview – Mark Bowden/Margaret Votava
- Readout and controls electronics – Mark Bowden
- Readout and controls software – Margaret Votava

Backup Slides

L1 Pixel Trigger Prototype Modules (P0)

L1 Pixel Trigger Prototype (P0 = Prototype)

- Preproc_P0 - Pixel Preprocessor
- SegTrk_P0 - Segment Tracker
- L1BufLnk_P0 - L1 Buffer Readout Link
- OptRec_P0 - Optical Receiver
- SegXLnk_P0 - Segment Tracker Interconnection Link
- SegSwi_P0 - Segment Tracker to Switch Link
- SegPTSM_P0 - Pixel Preprocessor and Segment Tracker PTSM
- SegPrw_P0 - Pixel Preprocessor and Segment Tracker Power & Enclosure

- SwiSeg_P0 - Switch to Segment Tracker Link
- SwiLogic_P0 - Switch Logic
- SwiXLnk_P0 - Switch Interconnection
- SwiFarm_P0 - Switch to Farm Link
- SwiXRLnk_P0 - Switch Rack Interconnection Link
- SwiPTSM_P0 - Switch PTSM

- Farmlet_P0 - Farm Motherboard
- FarmDau_P0 - Farm Daughter Card
- FarmSwi_P0 - Farm to Switch Link
- FarmLnk_P0 - Farm L1 Buffer Readout Link
- FarmGL1_P0 - Global L1 Result Link
- FarmPTSM_P0 - Farm PTSM
- FarmPwr_P0 - Farm Power & Enclosure
- FarmTst_P0 - Farm Test Stand

L1 Pixel Trigger Pilot Modules (P1)

L1 Pixel Trigger Pilot (P1 = Pilot)

- Preproc_P1 - Pixel Preprocessor
- SegTrk_P1 - Segment Tracker
-
- OptRec_P1 - Optical Receiver
- SegXLnk_P1 - Segment Tracker Interconnection Link
- SegSwi_P1 - Segment Tracker to Switch Link
- SegPTSM_P1 - Pixel Preprocessor and Segment Tracker PTSM
- SegPrw_P1 - Pixel Preprocessor and Segment Tracker Power & Enclosure

- Farmlet_P1 - Farm Motherboard
- FarmDau_P1 - Farm Daughter Card
- FarmSwi_P1 - Farm to Switch Link
-
- FarmGL1_P1 - Global L1 Result Link
- FarmPTSM_P1 - Farm PTSM
- FarmPwr_P1 - Farm Power & Enclosure
- FarmTst_P1 - Farm Test Stand

L1 Pixel Trigger Production Modules (P2)

L1 Pixel Trigger Production (P2 = Production)

- Preproc_P2 - Pixel Preprocessor
- SegTrk_P2 - Segment Tracker
- L1BufLnk_P2 - L1 Buffer Readout Link
- OptRec_P2 - Optical Receiver
- SegXLnk_P2 - Segment Tracker Interconnection Link
- SegSwi_P2 - Segment Tracker to Switch Link
- SegPTSM_P2 - Pixel Preprocessor and Segment Tracker PTSM
- SegPrw_P2 - Pixel Preprocessor and Segment Tracker Power & Enclosure

- SwiSeg_P2 - Switch to Segment Tracker Link
- SwiLogic_P2 - Switch Logic
- SwiXLnk_P2 - Switch Interconnection
- SwiFarm_P2 - Switch to Farm Link
- SwiXRLnk_P2 - Switch Rack Interconnection Link
- SwiPTSM_P2 - Switch PTSM

- Farmlet_P2 - Farm Motherboard
- FarmDau_P2 - Farm Daughter Card
- FarmSwi_P2 - Farm to Switch Link
- FarmLnk_P2 - Farm L1 Buffer Readout Link
- FarmGL1_P2 - Global L1 Result Link
- FarmPTSM_P2 - Farm PTSM
- FarmPwr_P2 - Farm Power & Enclosure
- FarmTst_P2 - Farm Test Stand

Global L1 Modules (P0 & P2)

GL1 Prototype (P0 = Prototype)

- GL1Farmlet_P0 - GL1 Farm Motherboard
- GL1FarmDau_P0 - GL1 Farm Daughter Card
- GL1FrontEnd_P0 - GL1 Front-End Electronics Interface
- GL1BufLnk_P0 - GL1 L1 Buffer Readout Link
- GL1ResLnk_P0 - GL1 Result Link
- GL1PTSM_P0 - GL1 Supervisor & Monitor
- GL1Pwr_P0 - GL1 Power & Enclosure

GL1 Production (P2 = Production)

- GL1Farmlet_P2 - GL1 Farm Motherboard
- GL1FarmDau_P2 - GL1 Farm Daughter Card
- GL1FrontEnd_P2 - GL1 Front-End Electronics Interface
- GL1BufLnk_P2 - GL1 L1 Buffer Readout Link
- GL1ResLnk_P2 - GL1 Result Link
- GL1PTSM_P2 - GL1 Supervisor & Monitor
- GL1Pwr_P2 - GL1 Power & Enclosure