BTeV Trigger and Data Acquisition System

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Overview

- Brief overview of the Trigger and Data Acquisition System (DAQ)

- WBS 1.8 – Trigger Electronics & Software
  - Project management overview
  - Architecture overview
  - Trigger R&D (used for cost and schedule estimates)
  - Response to Temple 2003 recommendations

- WBS 1.9 – Event Readout and Controls Electronics & Software
  - Project management overview
  - Major components of the DAQ
  - Response to the Temple 2003 recommendations

- Concluding remarks and list of presentations prepared for the Breakout Sessions

Introduction

- The challenge for the BTeV trigger and data acquisition system is to analyze particle tracks & interaction vertices for **EVERY** interaction that occurs in the BTeV detector, and to select interactions with *B* decays.

- The trigger performs this task using 3 stages, referred to as Levels 1, 2, and 3:
  "L1" – looks at every interaction, and rejects at least 98% of minimum bias background
  "L2" – uses L1 computed results & performs more refined analyses for data selection
  "L3" – performs a complete analysis using all of the data for an interaction

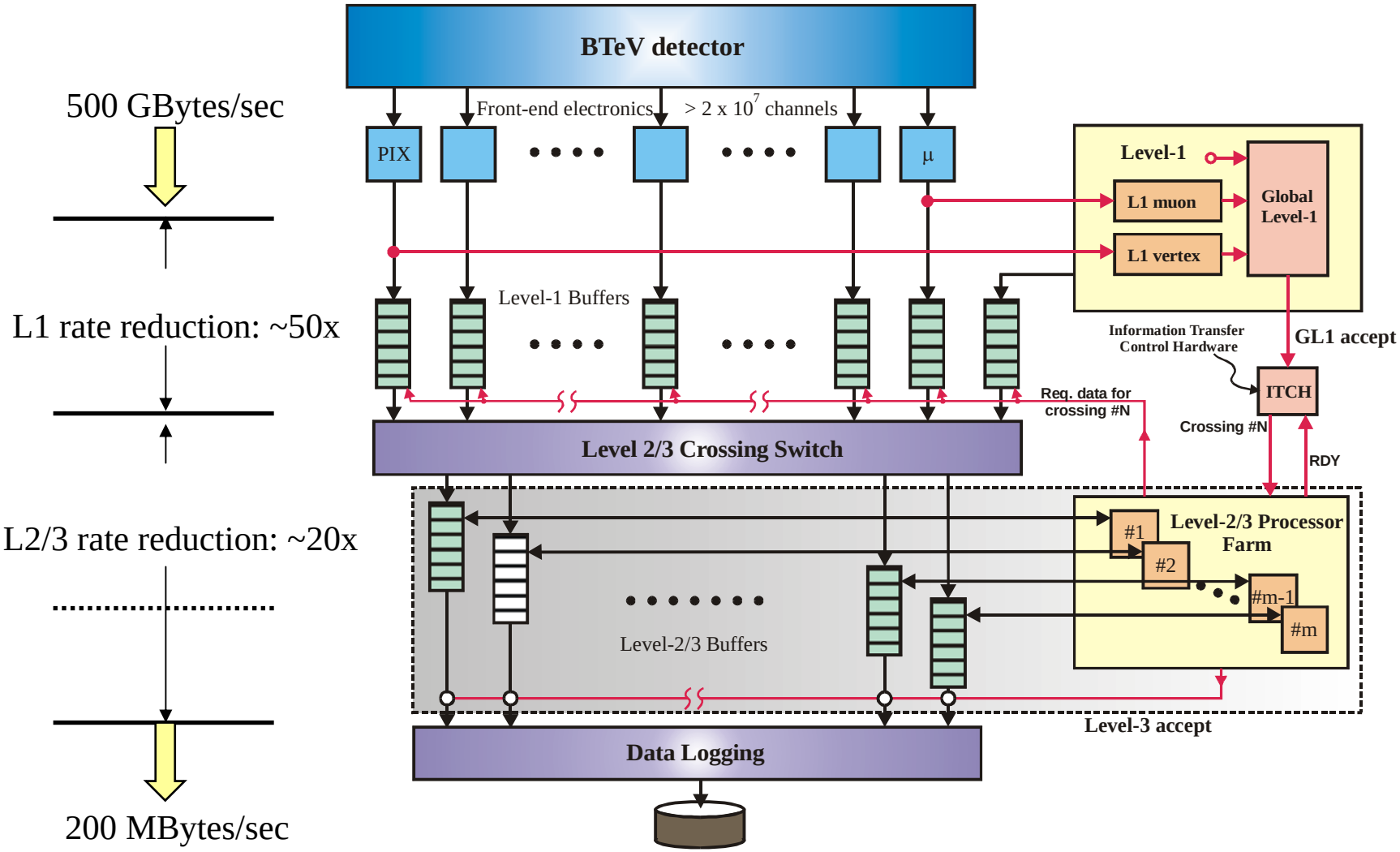
Reject > 99.9% of background. Keep > 50% of *B* events.

- The data acquisition system saves all of the data in memory for as long as is necessary to analyze each interaction (~ 1 millisecond on average for L1), and moves data to L2/3 processing units and archival data storage for selected interactions.

- The key ingredients that make it possible to meet this challenge:
  - BTeV pixel detector with its exceptional pattern recognition capabilities
  - Rapid development in technology – FPGAs, DSPs, microprocessors
  - Good ideas

FPGAs – field programmable gate arrays
DSPs – digital signal processors

Block Diagram of the BTeV Trigger & DAQ



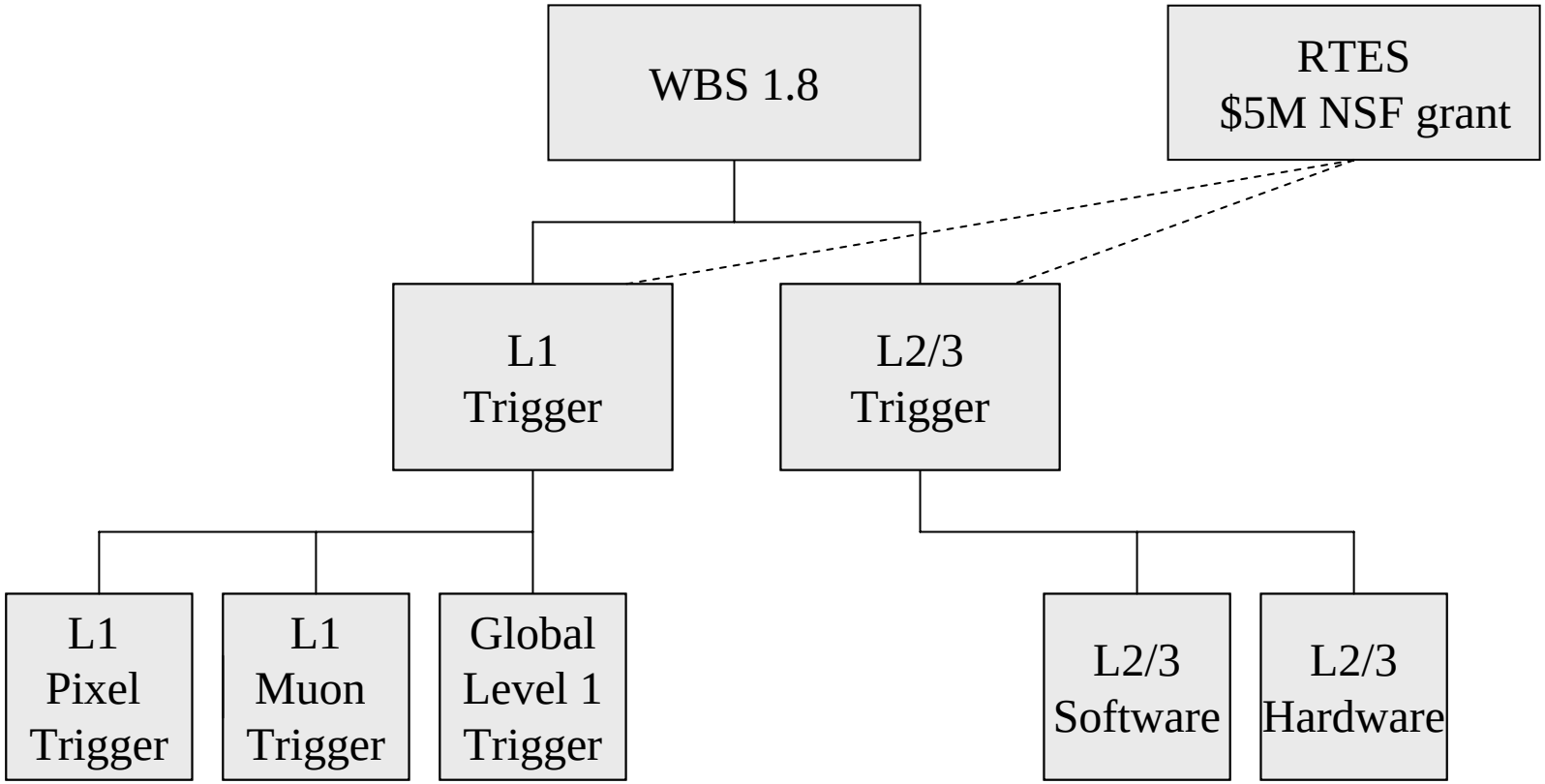
BTeV Trigger Components

- L1 pixel trigger (FPGAs, DSPs, L1 switch)
- L1 muon trigger (same hardware as L1 pixel trigger)
- Global Level 1 trigger (same DSP hardware)
- L2/3 hardware (Linux PC farm)
- L2/3 software (similar to HEP "offline" analysis)
- RTES software (fault detection and mitigation)

Base cost: $12.0M (Material: $6.9M, Labor: $5.1M)
+ $5M grant for RTES (NSF ITR program)

BTeV Trigger Electronics & Software

Base cost: $12.0M (Material: $6.9M, Labor: $5.1M)



BTeV Trigger Electronics & Software

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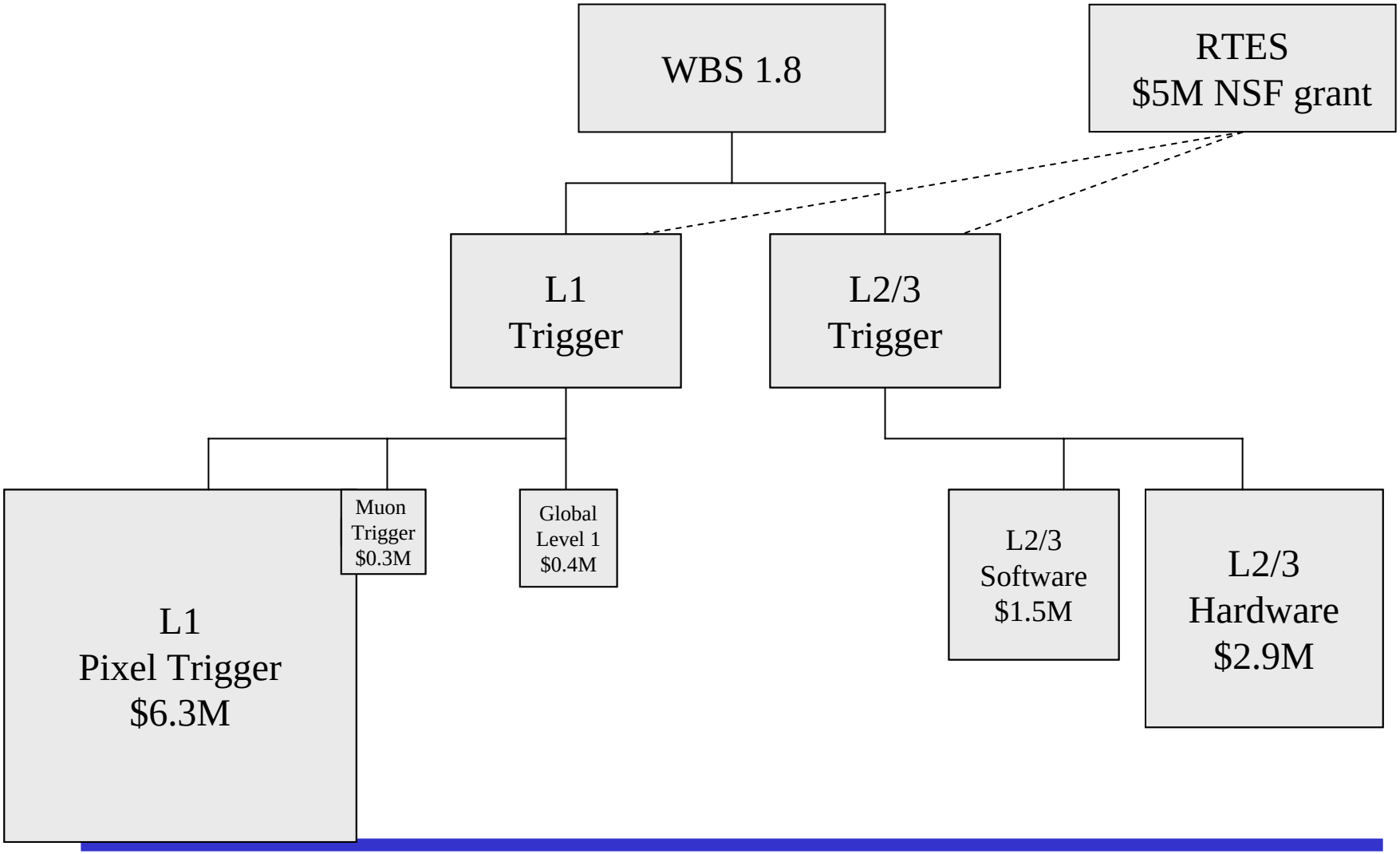
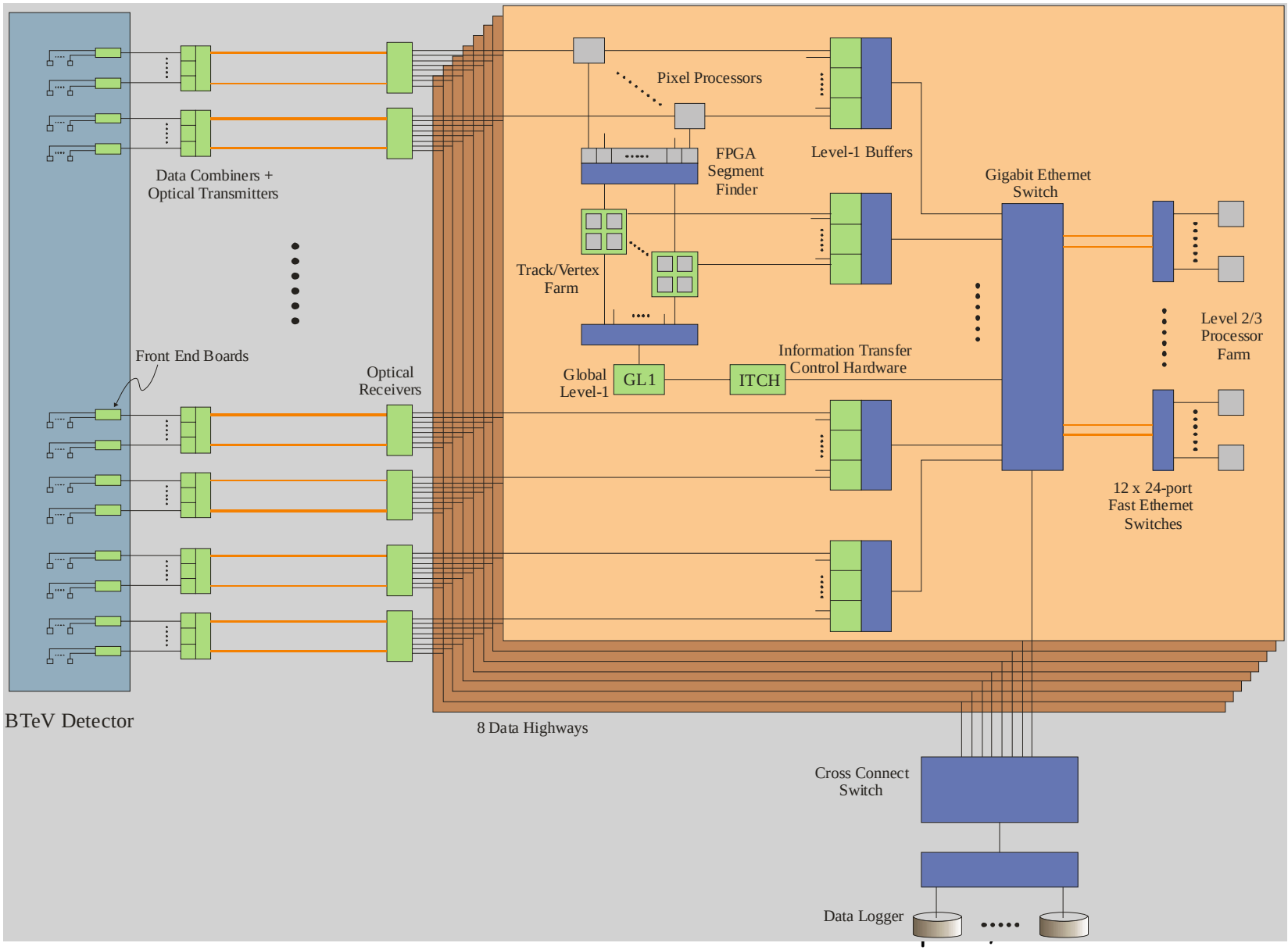
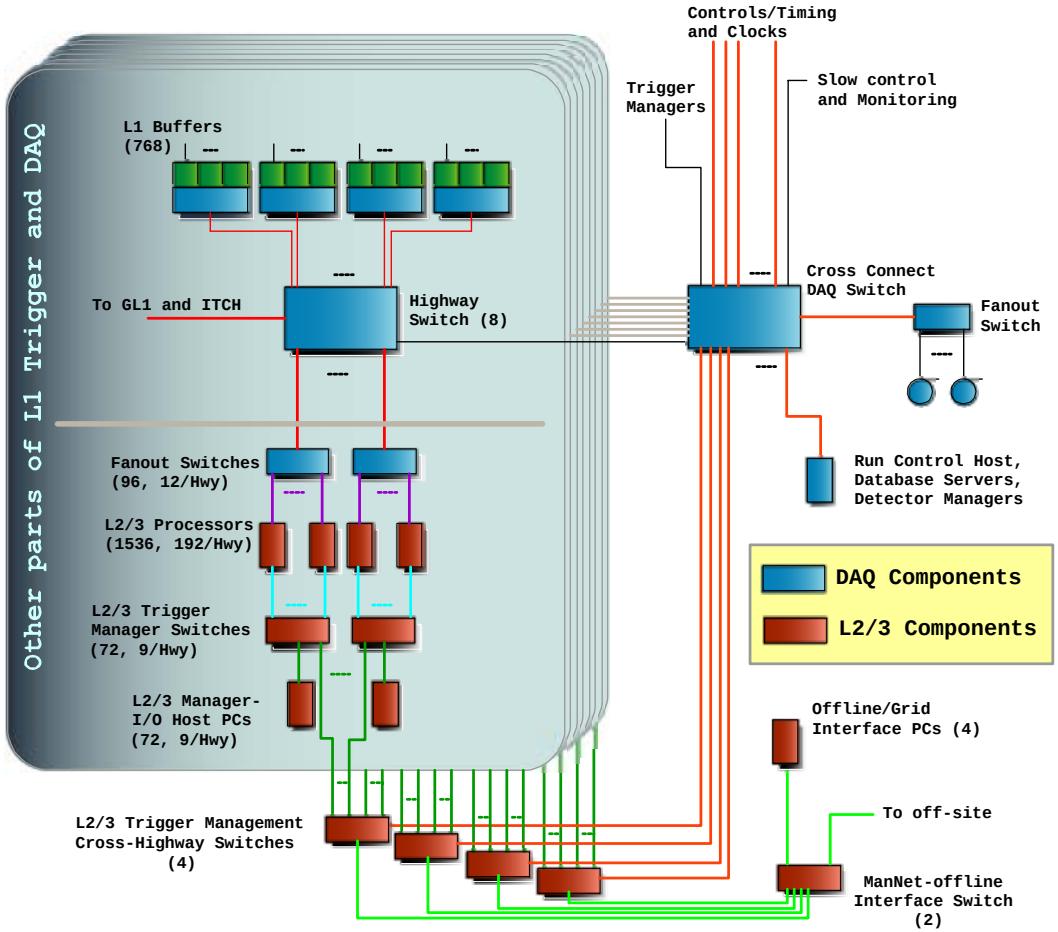


Three-level, eightfold trigger/DAQ architecture



L2/3 Trigger Hardware

Highway-Network View



Baseline Design

- L2/3 Processor farm consists of 1536 "12 GHz" CPUs (dual-CPU 1U rack-mount PCs)
- L2/3 Trigger also includes Manager-I/O Host PCs for database caches, worker management, monitoring, and event pool cache
- L2/3 Hardware in

L2 and L3 Trigger Software

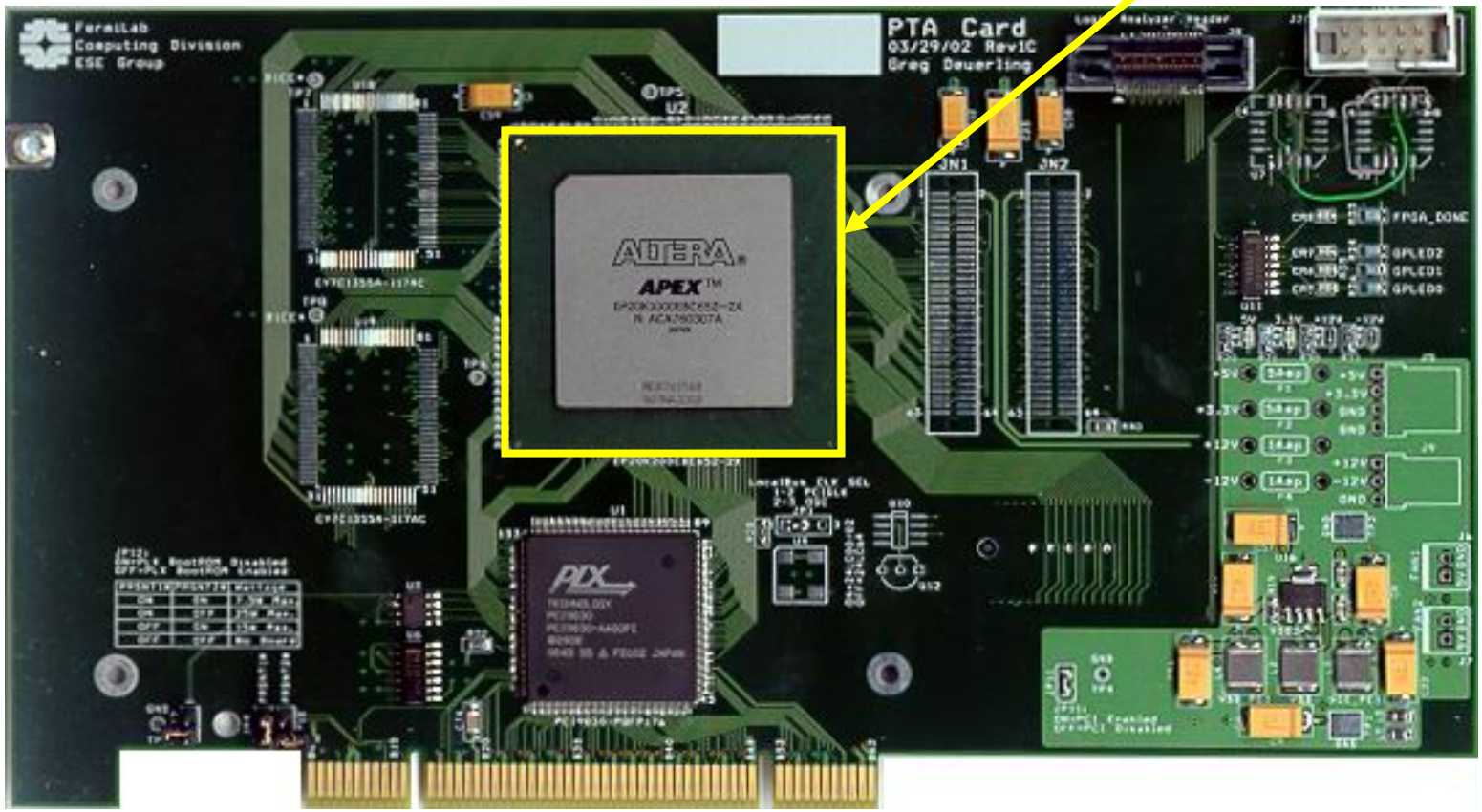
- L2 and L3 reconstruction software (tracks, photons, π^0's, Vees, particle ID, etc.)
- L2 and L3 trigger algorithms (selection criteria)
- Global L2 and Global L3 software (combinations of selection criteria and trigger lists)
- Alignment and Calibration software
- Monitoring and event display software
- Software framework utilities and interfaces to databases
- DAQ interface software (interfaces to actual DAQ hardware)
- Trigger specific system software (run control, control and monitoring, and databases)
- "L4" offline filter and fast charm/beauty monitoring software (specific selection and monitoring software needed before full L2/3 operational)

Trigger R&D (used for cost & schedule estimates)

- The FPGA segment-tracker algorithm (L1 pattern recognition) has been implemented on an Altera FPGA. This validates the segment-finding algorithm, and provides a basis for cost estimates (see next slide).
- Queuing simulations have been performed to address concerns raised by the June 2000 Technical Review of the BTeV trigger. Queue sizes and communication-channel bandwidths are within reasonable margins.
- A 4-DSP prototype system has been built to validate the design of the L1 DSP farm, and to determine costs associated with this part of the trigger.
- DSP timing studies have been performed for L1 pixel and L1 muon trigger algorithms on a Texas Instruments C6711 floating-point DSP. This provides a basis for cost estimates.
- A hash sorter has been developed to move some DSP calculations to an FPGA that is already included in the current design. Furthermore, an FPGA segment matcher is being investigated to move additional DSP calculations to an FPGA.
- Studies of alternative processors (e.g. Pentium and PowerPC processors) have been performed. Results suggest that alternative processors exceed estimates presented in the BTeV Proposal and Technical Design Report (TDR) by factors of 2 or 3 in performance.
- An RTES demonstration system (hardware and software) has been developed and was presented at Super Computing 2003. The system consists of initial prototypes of RTES deliverables (GME models, ARMORs, and VLAs).

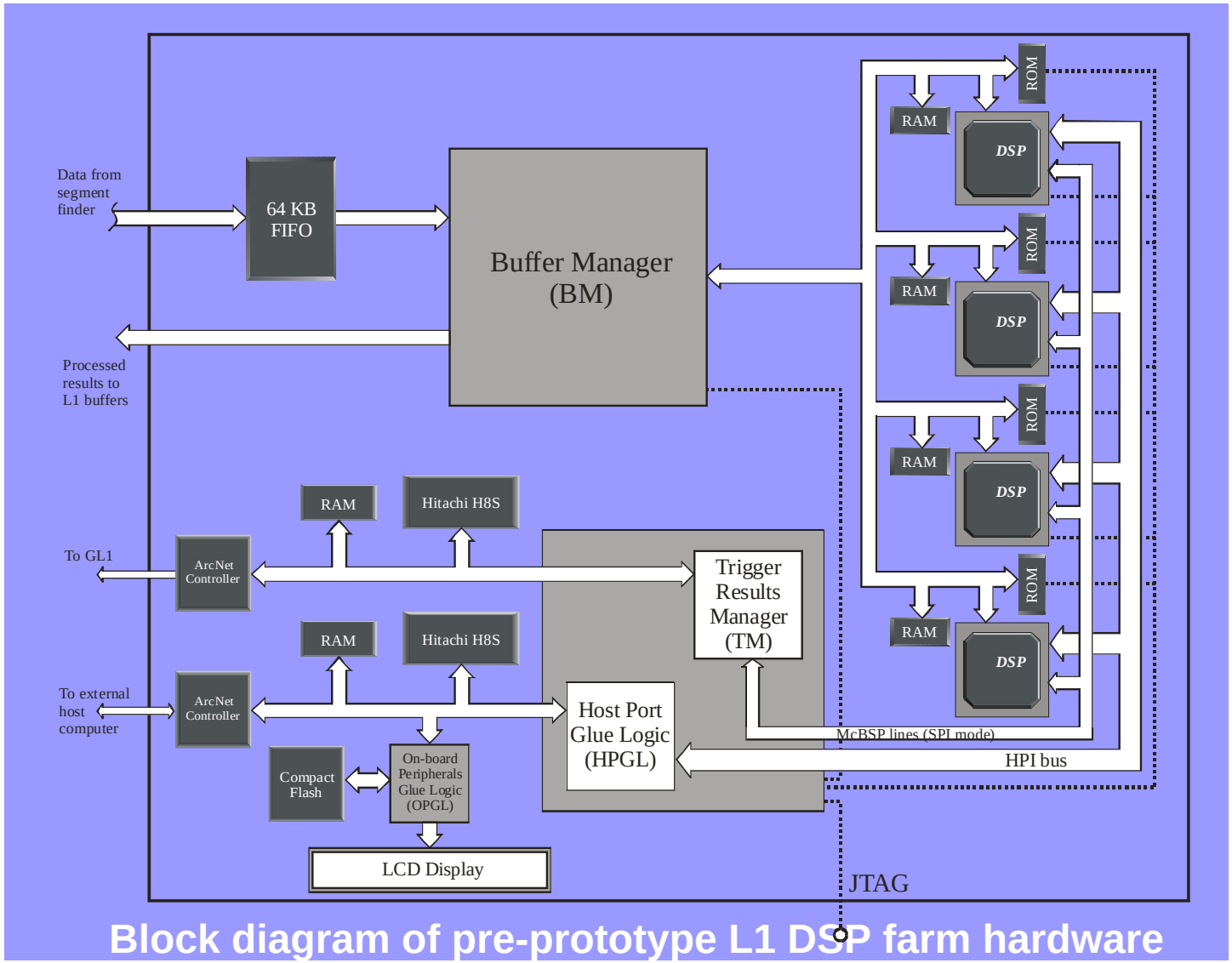
FPGA Segment Tracker R&D

Uses Altera APEX EPC20K1000 instead of EP20K200 on regular PTA



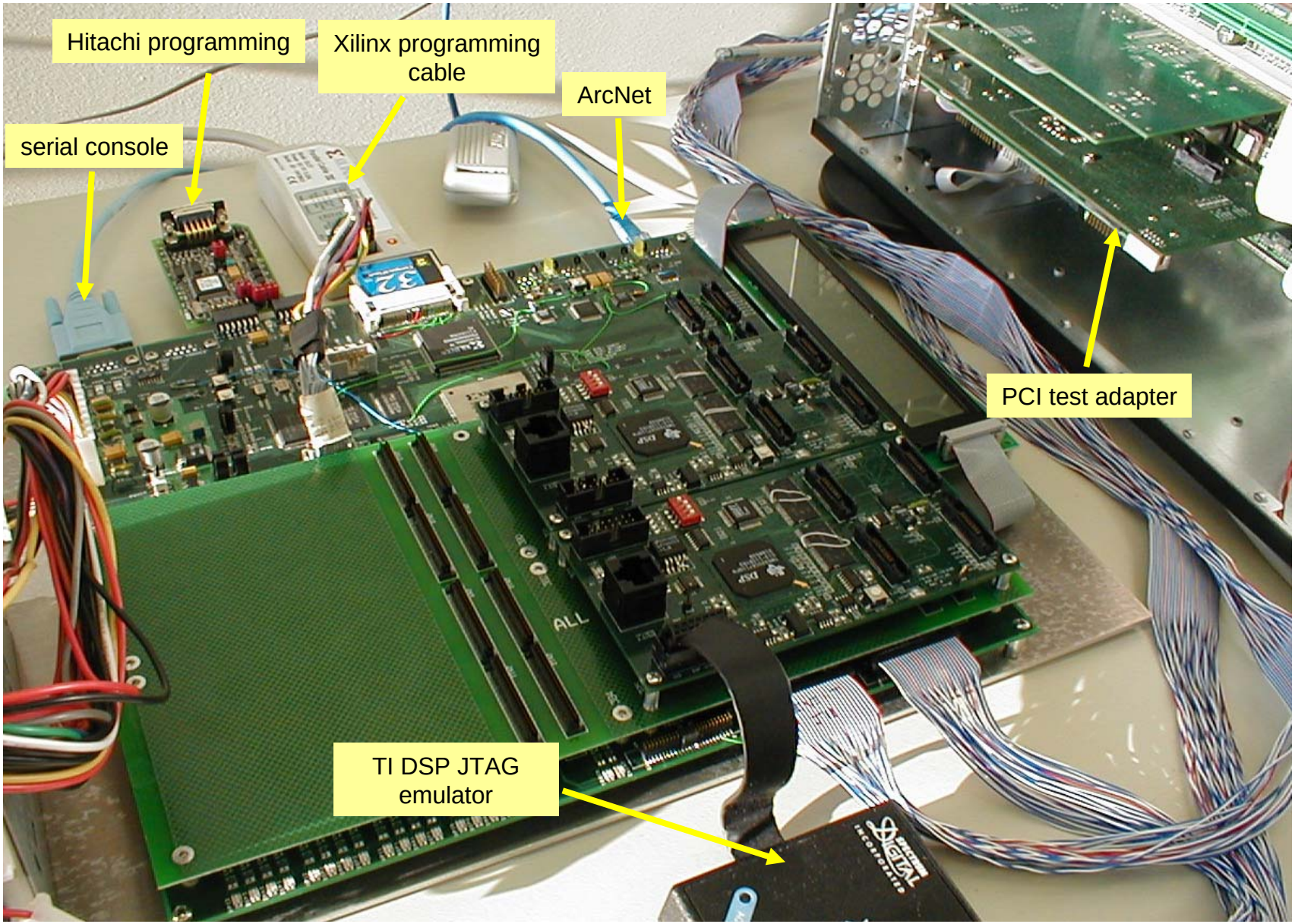
Modified version of PCI Test Adapter (PTA) card developed at Fermilab for testing hardware implementation of FPGA segment tracker (a.k.a. “Super PTA”)

L1 DSP Farm R&D



Block diagram of pre-prototype L1 DSP farm hardware

L1 Pre-prototype Test Stand

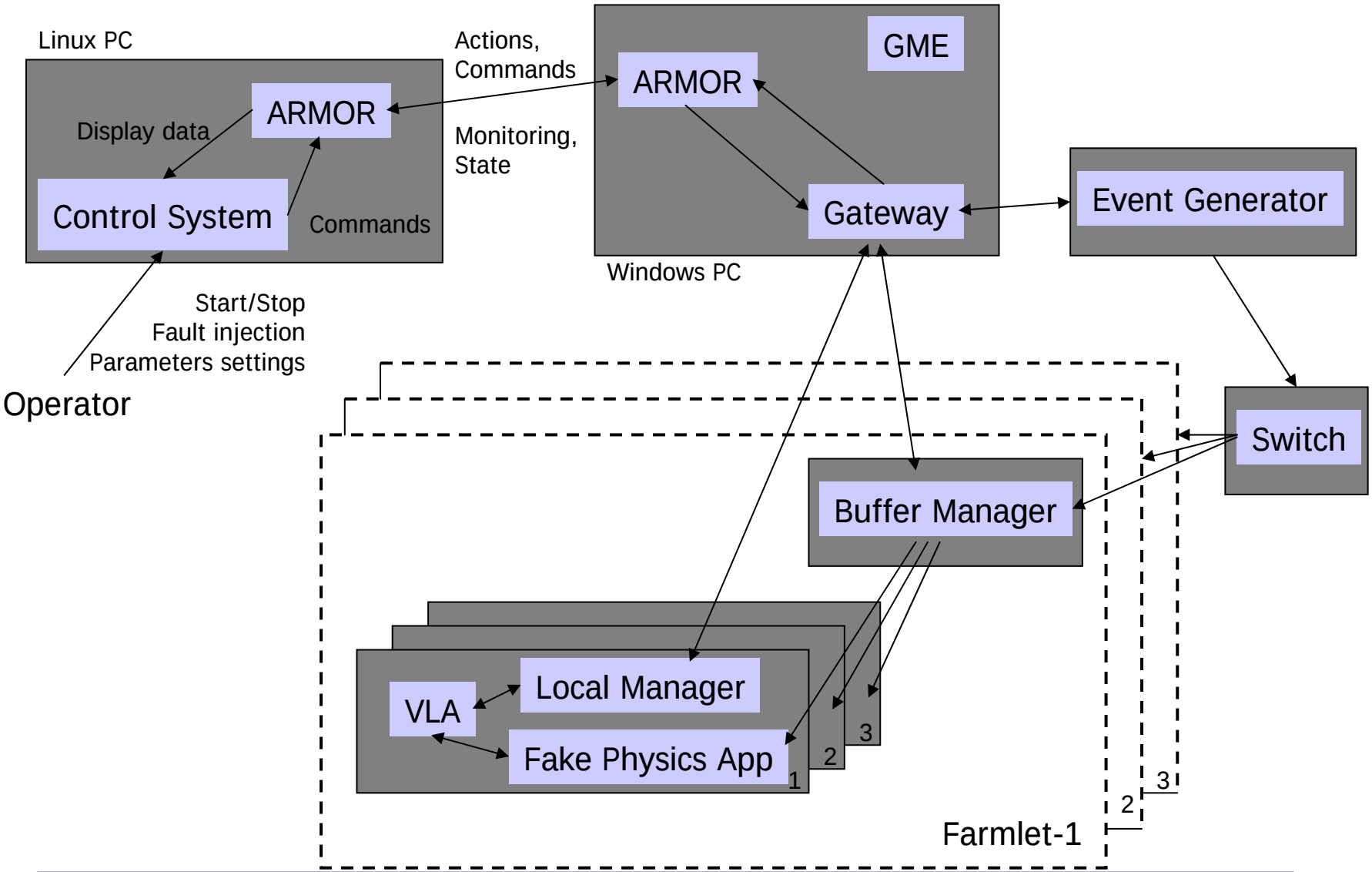


Size & Speed of L1 Muon Trigger Code

- Work done at UIUC
  - Implemented "clock-cycle" counting technique for timing tests.
  - Optimized muon trigger code (used for simulations) for DSP
  - Achieved DSP results for efficiency & rejection that satisfy requirements
  - The results support the cost estimates for the L1 muon trigger

TMS320C6711

RTES demonstration for Super Computing 2003



Temple Review 2003 WBS 1.8 (1 of 2)

- Recommendation 1: Describe the Level 1 Switch in the TDR asap.
  - A description of the L1 Switch is now in the TDR.
- Recommendation 2: Develop a prototype Level 1 Switch and a test setup to simulate realistic conditions.
  - The development of a "pre-pilot" Level 1 switch is part of our FY06 plan. Limited resources prevent us from doing this earlier.
- Recommendation 3: Continue the pursuit of alternate processor solutions for the track and vertex processors, and build corresponding prototype daughter cards.
  - The development of a "pre-pilot" farmlet is planned for FY05. We will develop a complete system (hardware and software) and are currently working on studies of alternative embedded processors, alternative interconnect technologies, real-time operating systems, evaluation of a message-passing system, and evaluation of RTES deliverables for control and monitoring.

Temple Review 2003 WBS 1.8 (2 of 2)

- Recommendation 4: Evaluate RTES tools promptly with prototype hardware (at all levels).
  - RTES tools have been evaluated by developing a Level 1 trigger prototype for Super Computing 2003. The development of a more extensive prototype is in the planning stage.
- Recommendation 5: (Strongly) encourage new institutions to contribute to the Level 3 filtering software....
  - We need to get new collaborators or new people from currently collaborating institutions to work on Level 3 software.
- Recommendation 6: Develop a preliminary staged plan for reduction of data size to permanent storage from the full raw data to DST....
  - We will establish a working group to study this and report later this year.

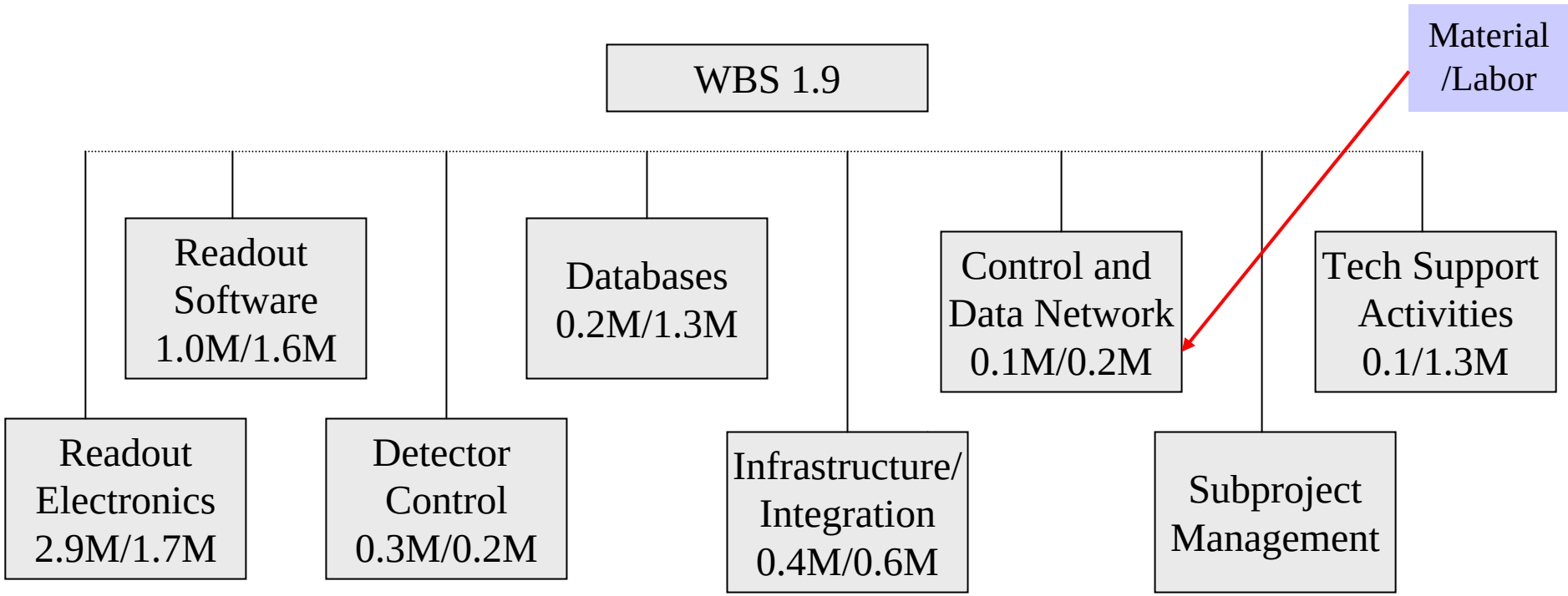
BTeV Readout and Controls (DAQ)

- Readout electronics
- Data acquisition software
- Detector control system
- Databases
- Control & data network
- Technical Support

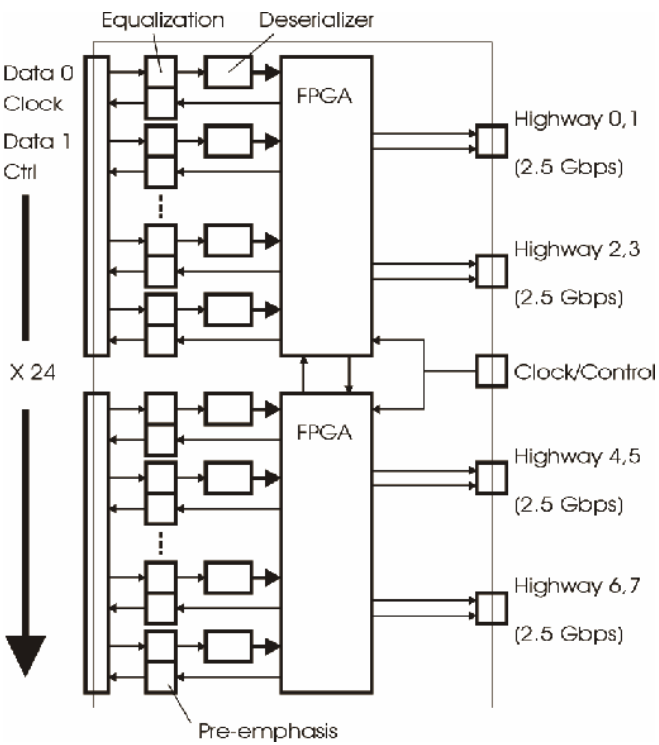
Base cost: $12M (Material: $5M, Labor: $7M)

WBS 1.9 – Readout, Controls Electronics & Software

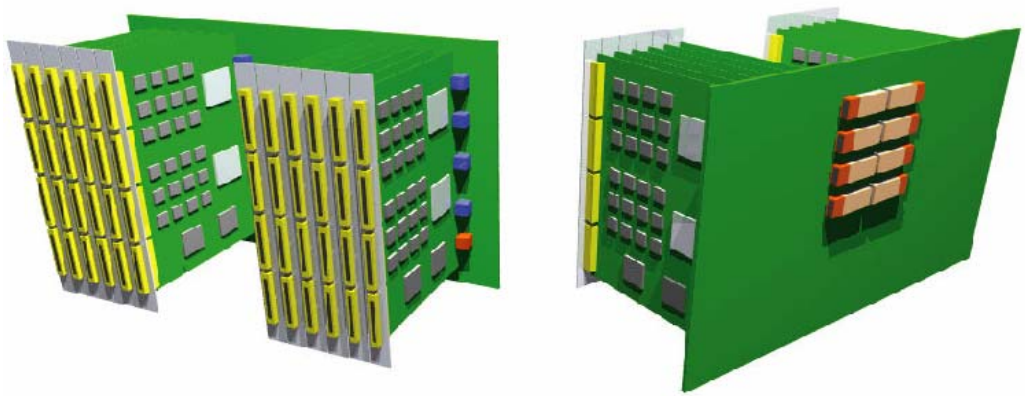
Base cost: $12M (Material: $5M, Labor: $7M)



Data Combiner Boards (DCBs)

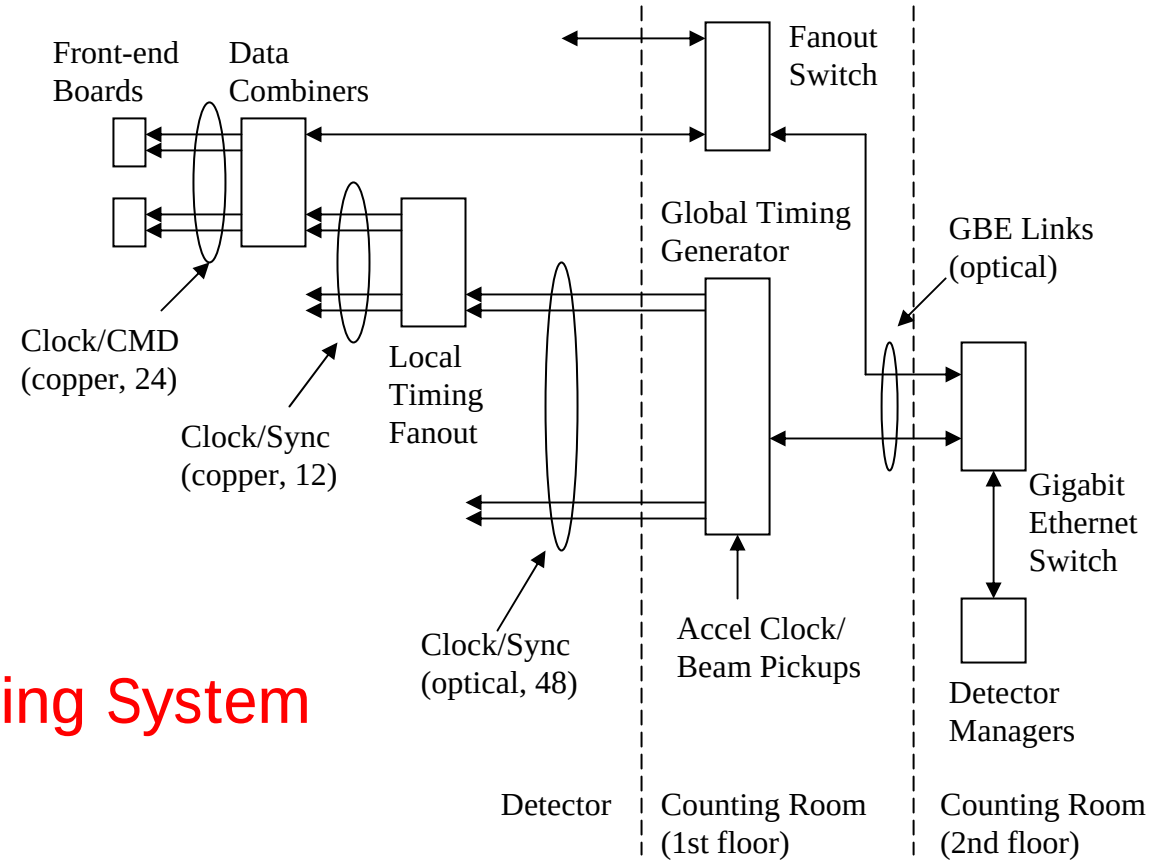


Data Combiner



Input receiver/multiplexer for all (non-triggered) detector front-end boards.

Timing System

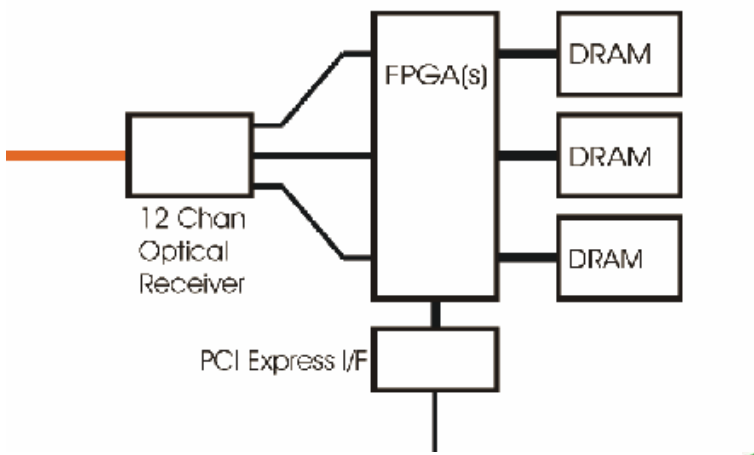


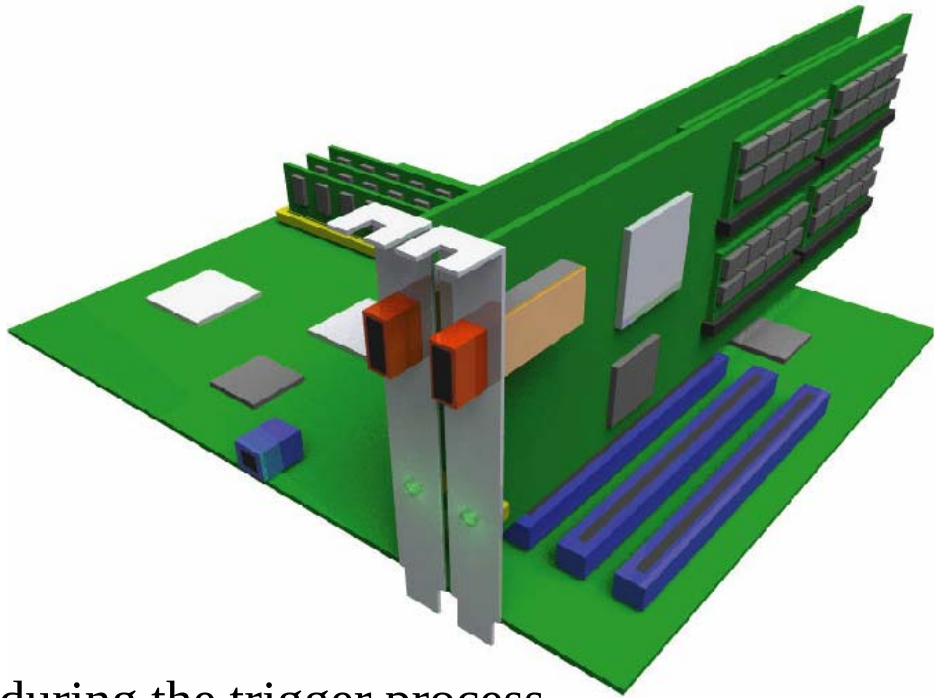
Timing System

Fast control and timing distribution network for precise system synchronization.

Level 1 Buffer

Update with new L1B prototype design



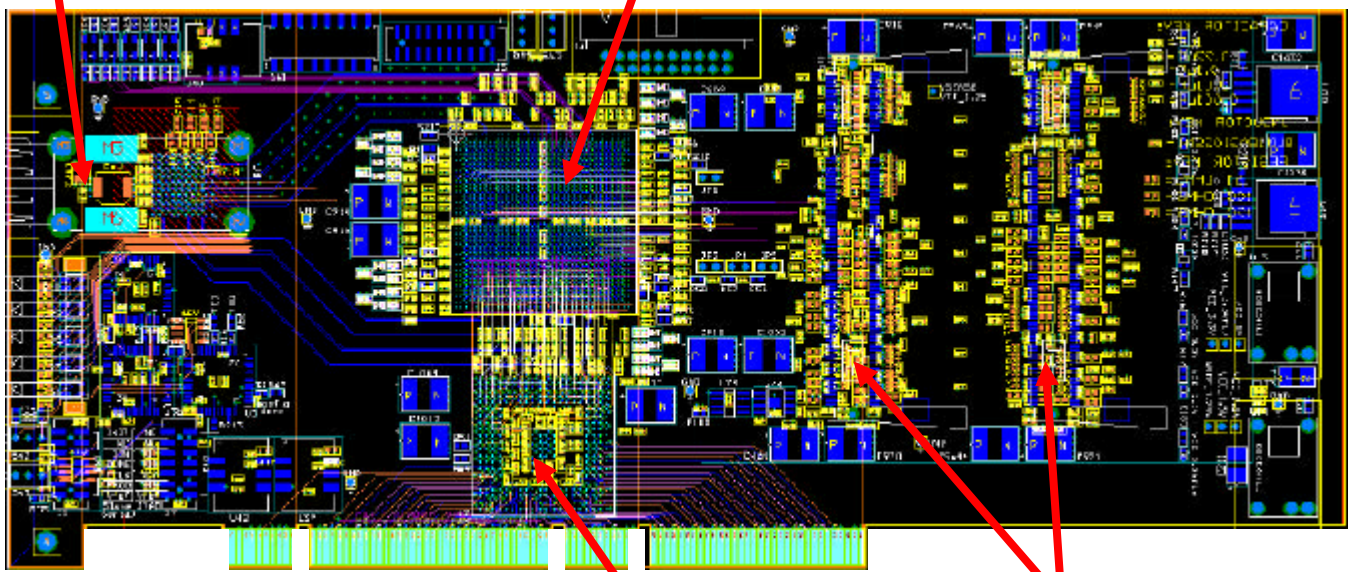


Large capacity buffers to hold data during the trigger process.

L1 Buffer Prototype

Optical Receiver (12 channels X 2.5 Gbps)

FPGA (deserializers, memory controller)

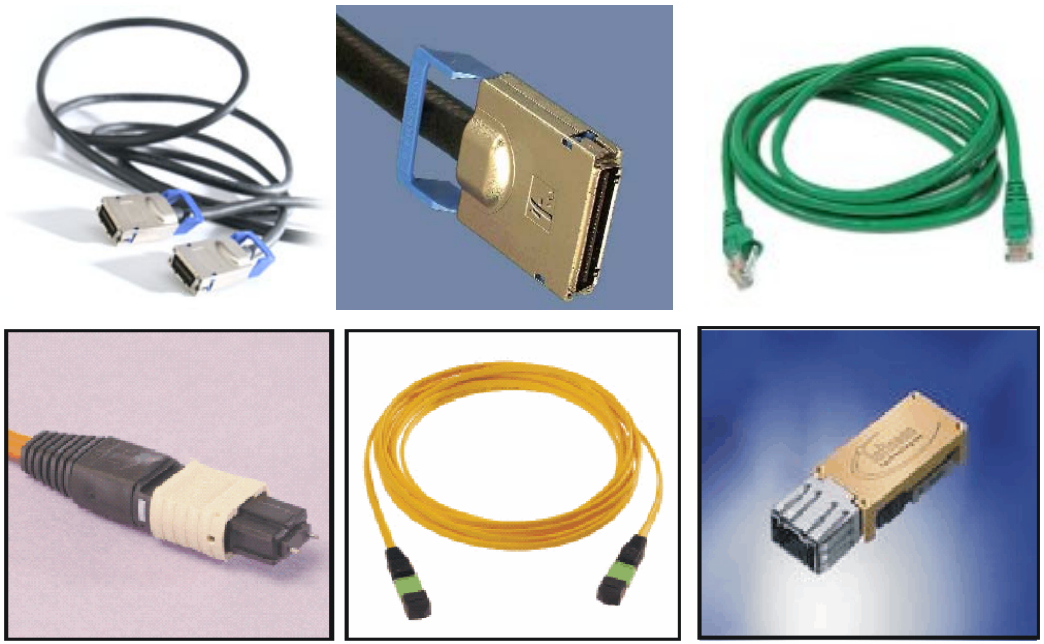


PCI Interface

DRAM (512 MB X 2, DDR SODIMM)

- Expect first boards in one month
- Standard optical interface
- Buffer memory architecture
- PCI Interface (BTeV will use a newer generation, maybe PCI-Express)

Data Links



Front-end to Data Combiners
- 600 Mbps copper

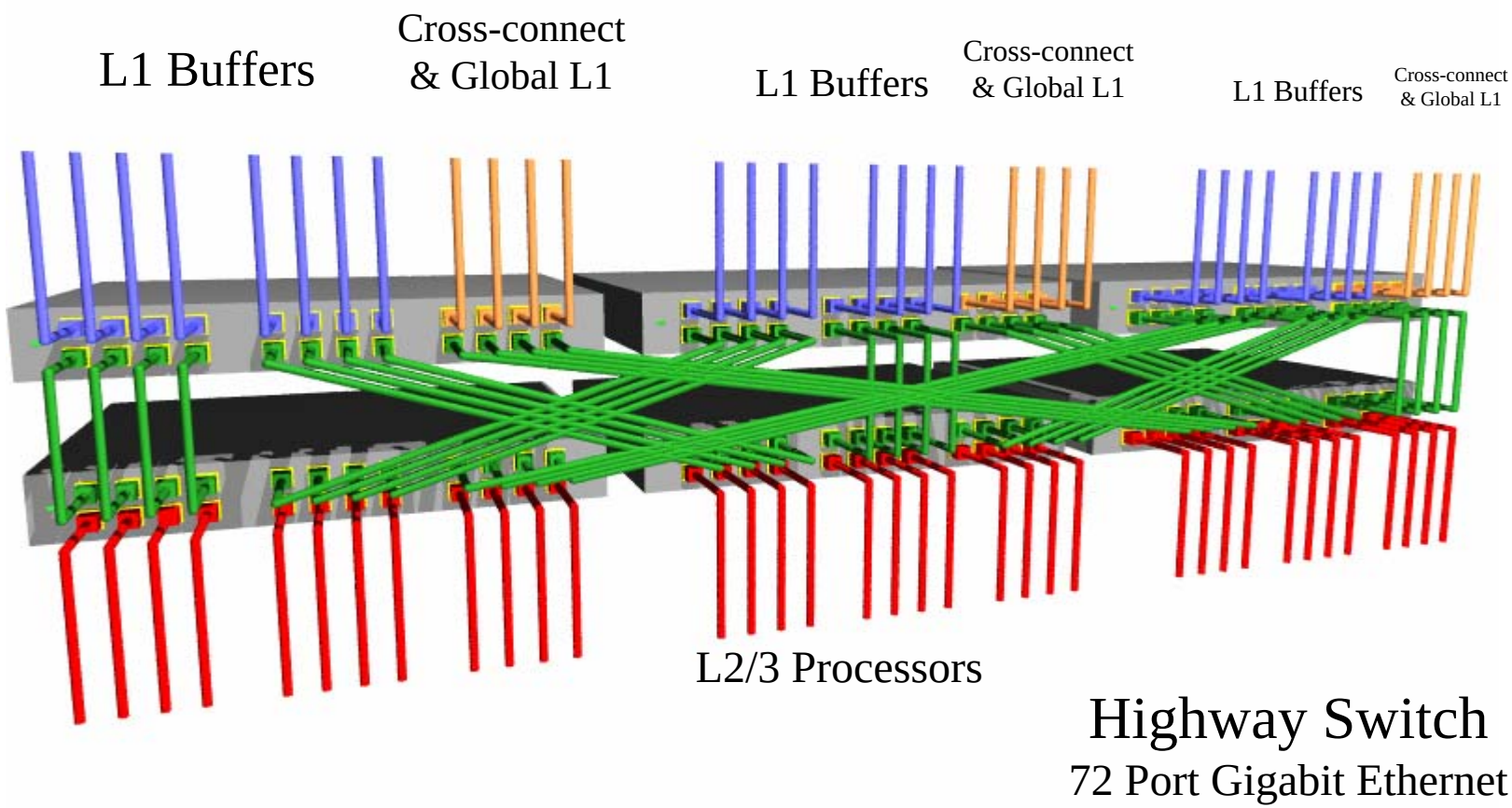
Data Combiners to L1 buffers & L1 Trigger
- 2.5 Gbps optical

L1 Trigger to L1 Buffers
- 2.5 Gbps copper

Network
- 1 Gbps (CAT6) copper

(all point-to-point serial)

Highway Switch (for a single data highway)



Other Major Components of WBS 1.9

- Configuration Subsystem - software to download, initialize and partition all system components
- Run Control Subsystem - software to control and monitor the operation and overall dataflow of the system
- Detector Control - "slow" control network to set and monitor all system environmental parameters
- Databases - store and access operating parameters, maintain a time history of all system variables, and store and access parameters necessary for trigger algorithms
- Infrastructure - counting and control room infrastructure

Temple Review 2003 WBS 1.9

- Recommendation 1: Develop a DCB prototype
  - The development of a DCB prototype will begin in Spring 2004. Since the last review, we have begun merging the DCB design for the pixel/silicon detectors with the DCB design used by other sub-detectors. Concerns that the development of the DCB prototype had to be delayed due to the DAQ funding profile have been addressed and initial support for this project will come from the pixel detector sub-project.
- Recommendation 2: Choose a clock distribution scheme and prototype the corresponding hardware. Investigate interactions with the various trigger and DAQ components
  - Our work with the Tevatron beam position monitor system allowed us to gain experience with the accelerator timing system. This led to some simplification of the BTeV timing system, as it appears likely that we will be able to re-use in BTeV some of the components developed for the BPM system. Details of the new design will be presented in the breakout sessions.

Temple Review 2003 WBS 1.9 cont'd

- Recommendation 3: Evaluate the radiation levels in the proposed DCB locations and their impact on DCB performance. Determine DCB location and verify adequate performance of the cables to the front-ends
  - Total radiation dose received by the DCB modules is not a major concern, since radiation levels at the default locations around the detector are less than 0.5KRad/yr (most integrated circuits can handle 20KRad or more). We are, however, concerned about single event upset, and we plan to implement some logic redundancy as well as continuously scrub (reload) the DCB FPGAs.
  - The performance of the data links (copper between detector and DCBs, optical between DCBs and L1 buffers) was studied several years ago. With a HP G-Link based system we obtained bit failure rates at the 10-15 level – sufficiently low for BTeV. We are planning to repeat these tests in the next months with the L1B prototype board which uses the same optical interface we intend to use for BTeV. For the links between the front-end electronics and the DCBs we will use shielded CAT 6 cables. Cat 5/6 cabling is currently used in StarGen interconnects at similar speeds and distances. The performance of these cables needs to be verified however. We listed this as a risk item and also assigned a 100% contingency to the front-end cable costs.

Trigger & DAQ Summary

- Our basic designs for both the trigger and DAQ have been stable since the BTeV Proposal (May 2000).
- The DAQ design is based on commercial networking equipment, which eliminates concerns about building a custom switch.
- The trigger system has a design that can accommodate new ideas, changes in running conditions, and new technology. The design includes FPGAs, DSPs, and PCs. We exploit the strengths of each type of hardware, and we can change our implementation as we learn more about running conditions and physics goals.
- For example: we have been studying two new ideas (hash sorting & segment matching) that promise to improve the L1 trigger design by moving DSP calculations to FPGAs that are already included in the design.
- Another example: we are considering alternatives to DSPs (such as Pentium and PowerPC processors) that could provide higher performance at Level 1 for lower cost.

Concluding Remarks

More information on the BTeV Trigger and DAQ is available in presentations that have been prepared for the breakout sessions.

WBS 1.8:

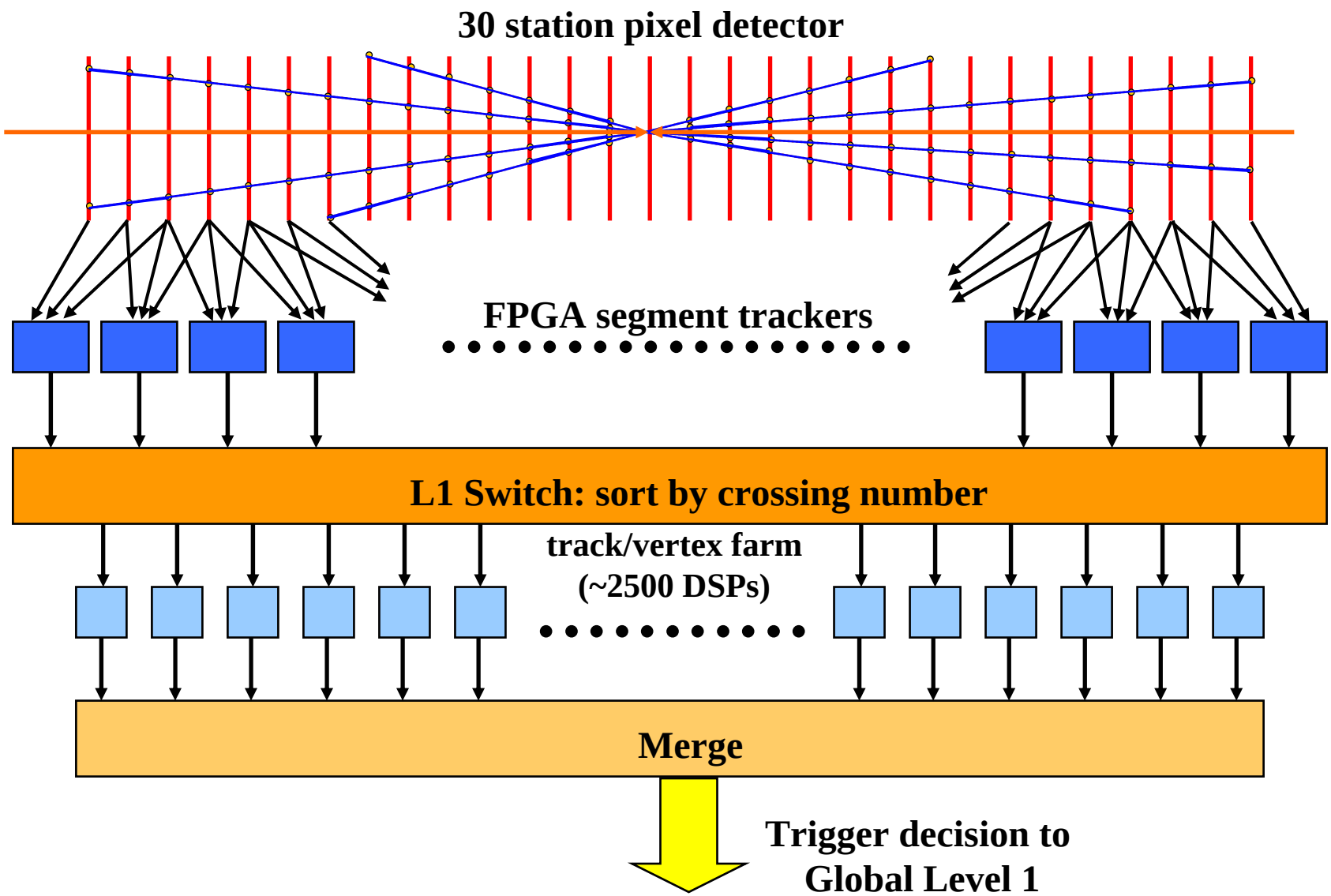
- Overview – Erik Gottschalk
- L1 pixel trigger – Gustavo Cancelo
- L1 muon trigger – Mike Haney
- L1 muon trigger algorithm – Mats Selen
- Global Level 1 – Vince Pavlicek
- L2/3 software – Paul Lebrun
- L2/3 hardware – Harry Cheung
- RTES – Jim Kowalkowski

WBS 1.9:

- Overview – Klaus Honscheid
- Readout and controls electronics – Mark Bowden
- Readout and controls software – Margaret Votava

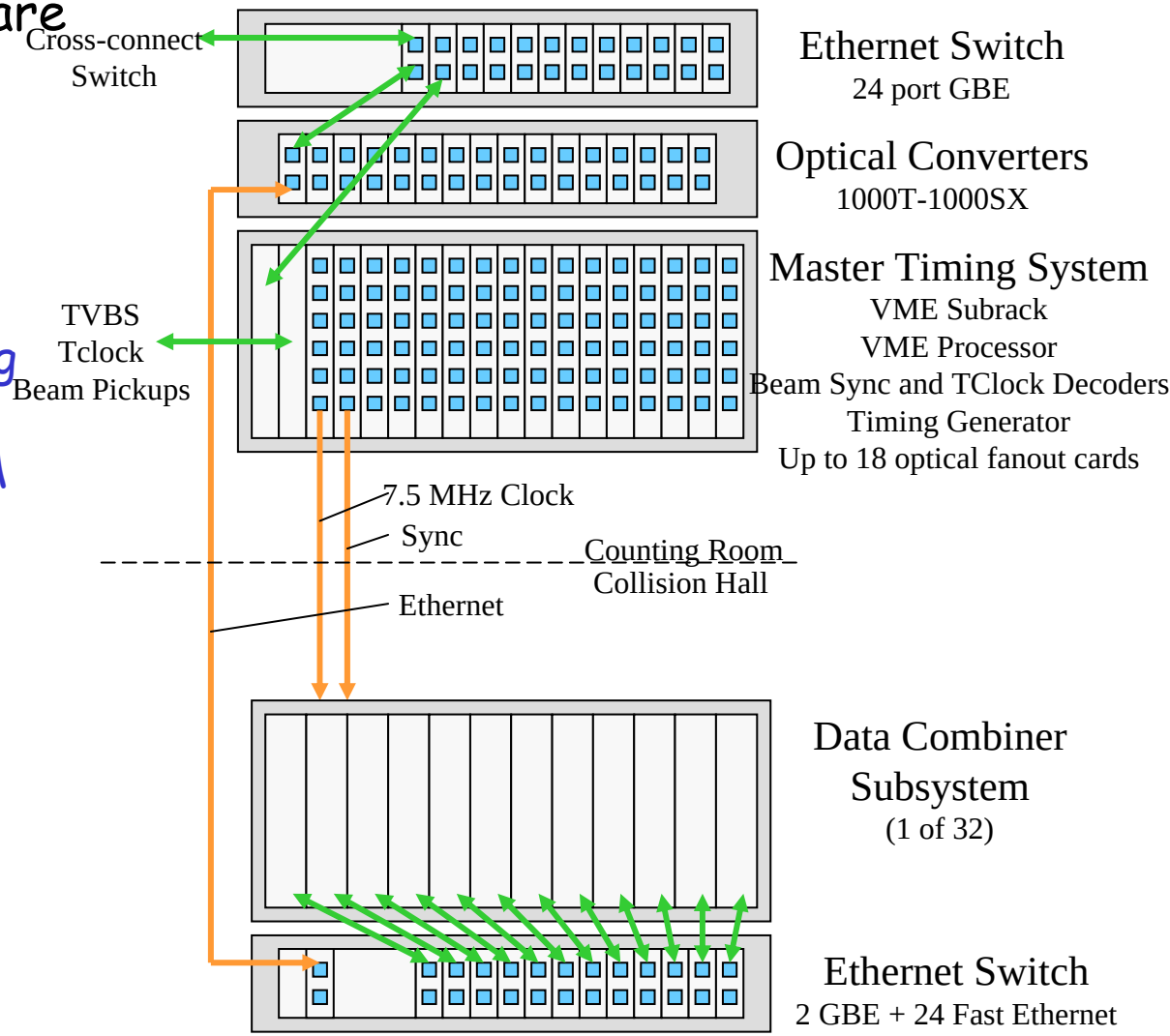
Backup Slides

L1 pixel trigger architecture



Timing System

- Generate and distribute signals synchronized with the accelerator clock
- 1 ns or better precision resolution/jitter
- 7.5 MHz clock and sync signals are delivered to each DCB subsystem.
- Control message (start/stop/calibrate) are sent asynchronously over Ethernet. Commands are activated at a predefined (bunch crossing) clock signal
- DCB modules perform fine-grain timing and clock phase adjustments (for each front-end link)
- Static timing information – e.g. bunch fill patterns – will be stored in the DCBs.
- Since the data is send from the detector to the DCBs on every crossing no fast trigger signal or other external timing information is required.

Timing System Implementation

- Use commercial hardware
  - VME (CPU, crate)
  - Ethernet switches
  - Optical converters
- Use existing hardware
  - Clock decoders, timing generators developed for the Tevatron BPM project.
- Optical fan-out cards are new but simple