BTeV Trigger (WBS 1.8)

Erik Gottschalk

Overview

- Introduction and overview of the BTeV trigger
- WBS 1.8 – Trigger electronics & software
  - Project description
  - Project organization
  - Technical details and progress since DOE CD-1 Review
  - Cost
  - Schedule
  - Milestones
  - Risk assessment
  - Response to DOE CD-1 recommendations
  - FY05 Project Plans and Status
- Presentations prepared for breakout sessions

Introduction

- The challenge for the BTeV trigger and data acquisition system is to reconstruct particle tracks and interaction vertices for **EVERY** interaction that occurs in the BTeV detector, and to select interactions with *B* decays.

- The trigger performs this task using 3 stages, referred to as Levels 1, 2, and 3:
  "L1" – looks at every interaction and rejects at least 98% of min. bias background
  "L2" – uses L1 computed results & performs more refined analyses for data selection
  "L3" – rejects additional background and performs data-quality monitoring

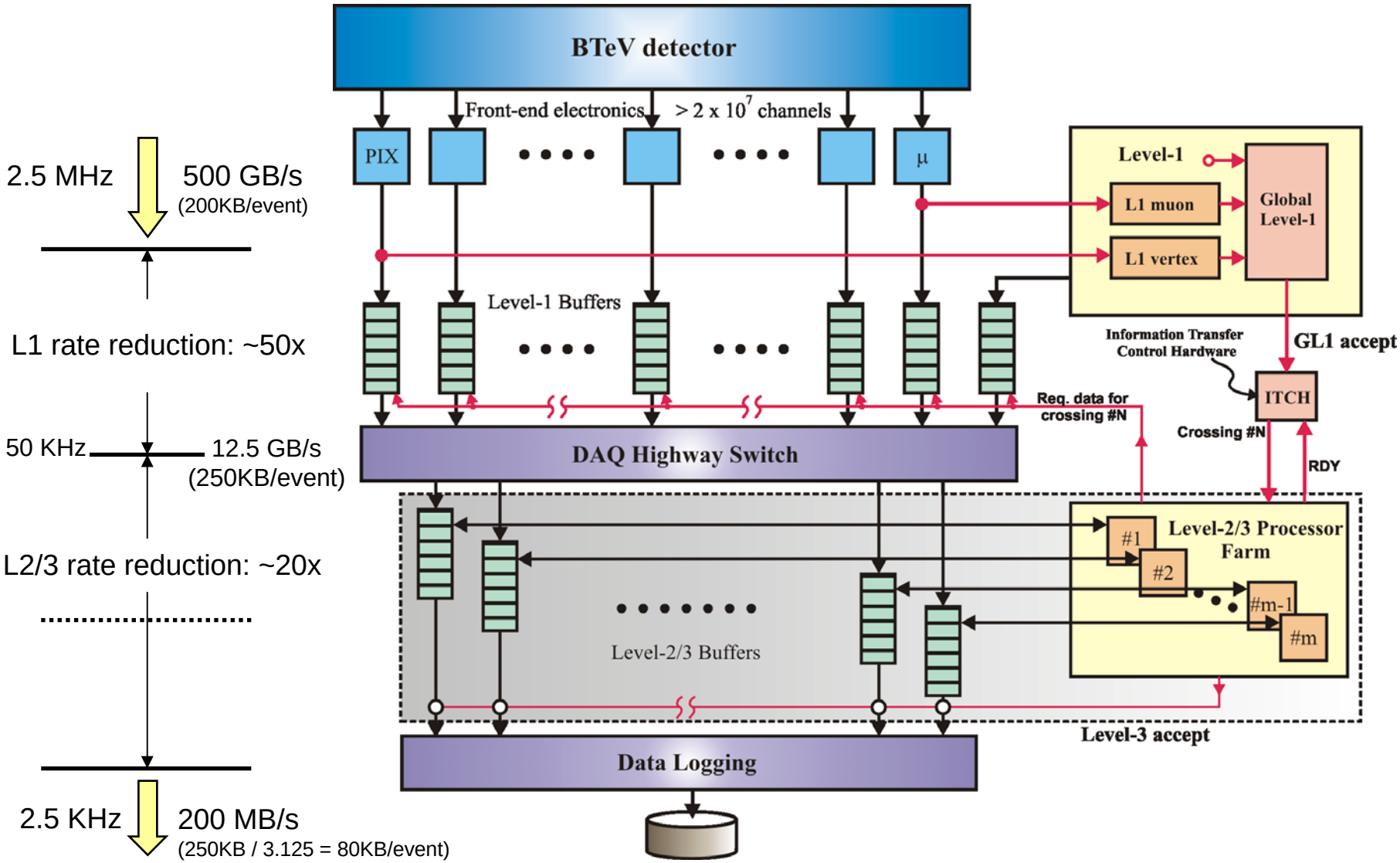
Reject > 99.9% of background. Keep > 50% of *B* events.

- The data acquisition system saves all of the data in memory for as long as necessary to analyze each interaction, and moves data to L2/3 processing units and archival data storage for selected interactions.

- The key ingredients that make it possible to meet this challenge:
  - BTeV pixel detector with its exceptional pattern recognition capabilities
  - Rapid development in technology – FPGAs, processors, networking

Note: see glossary at the end of this talk

Block Diagram of the Trigger & DAQ



Project Description WBS 1.8

- L1 pixel trigger (FPGAs, L1 Switch, L1 Farm)
- L1 muon trigger (same hardware as L1 pixel trigger)
- Global Level 1 trigger (same processing hardware)
- L2/3 hardware (Linux PC farm)
- L2/3 software (similar to HEP "offline" analysis)
- RTES software (fault detection and mitigation)

Base cost (FY05 dollars): $11.4M (Material: $7.8M, Labor: $3.6M)

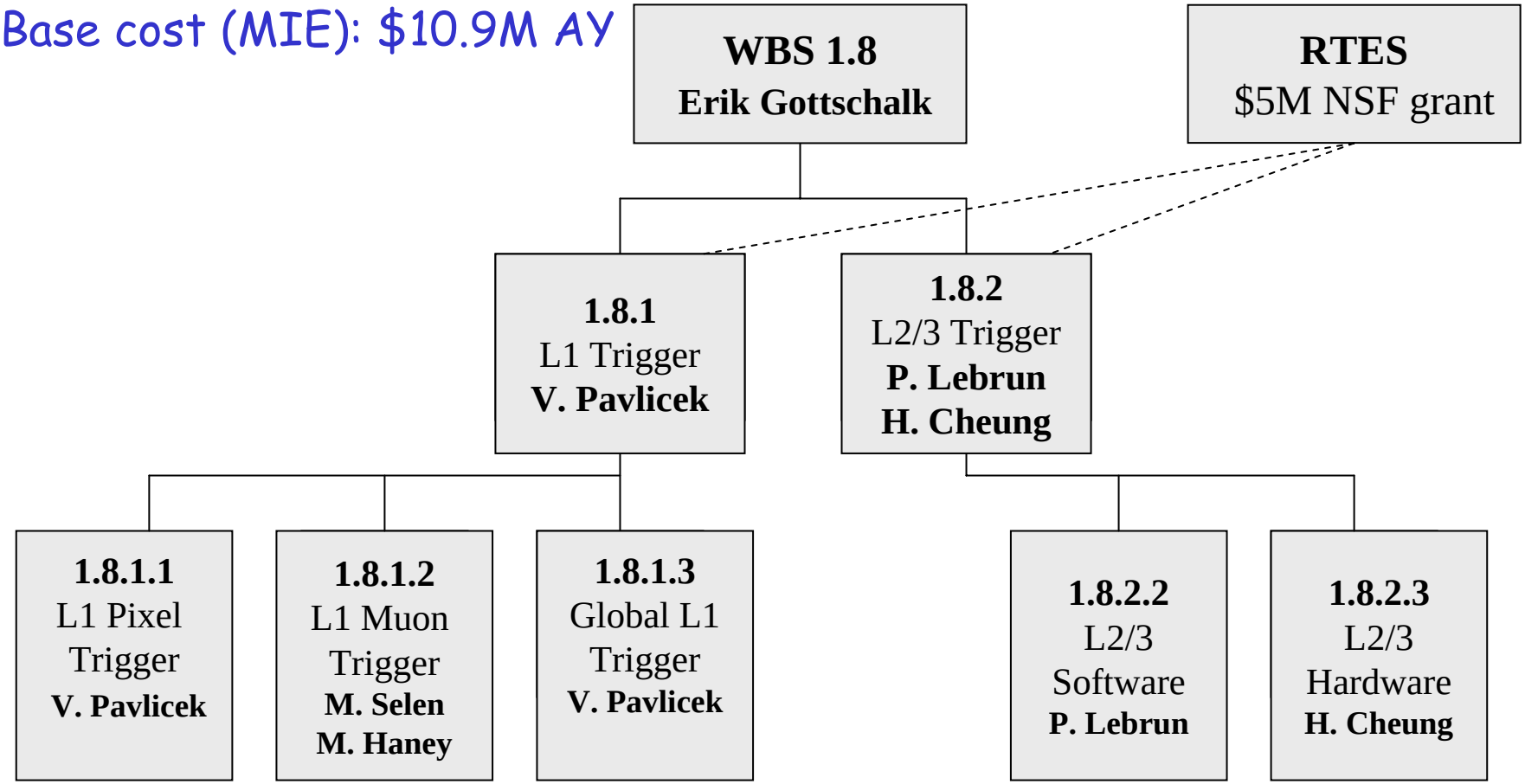
Base cost (MIE): $10.9M AY

+ $5M grant for RTES (NSF ITR program)

Organization WBS 1.8

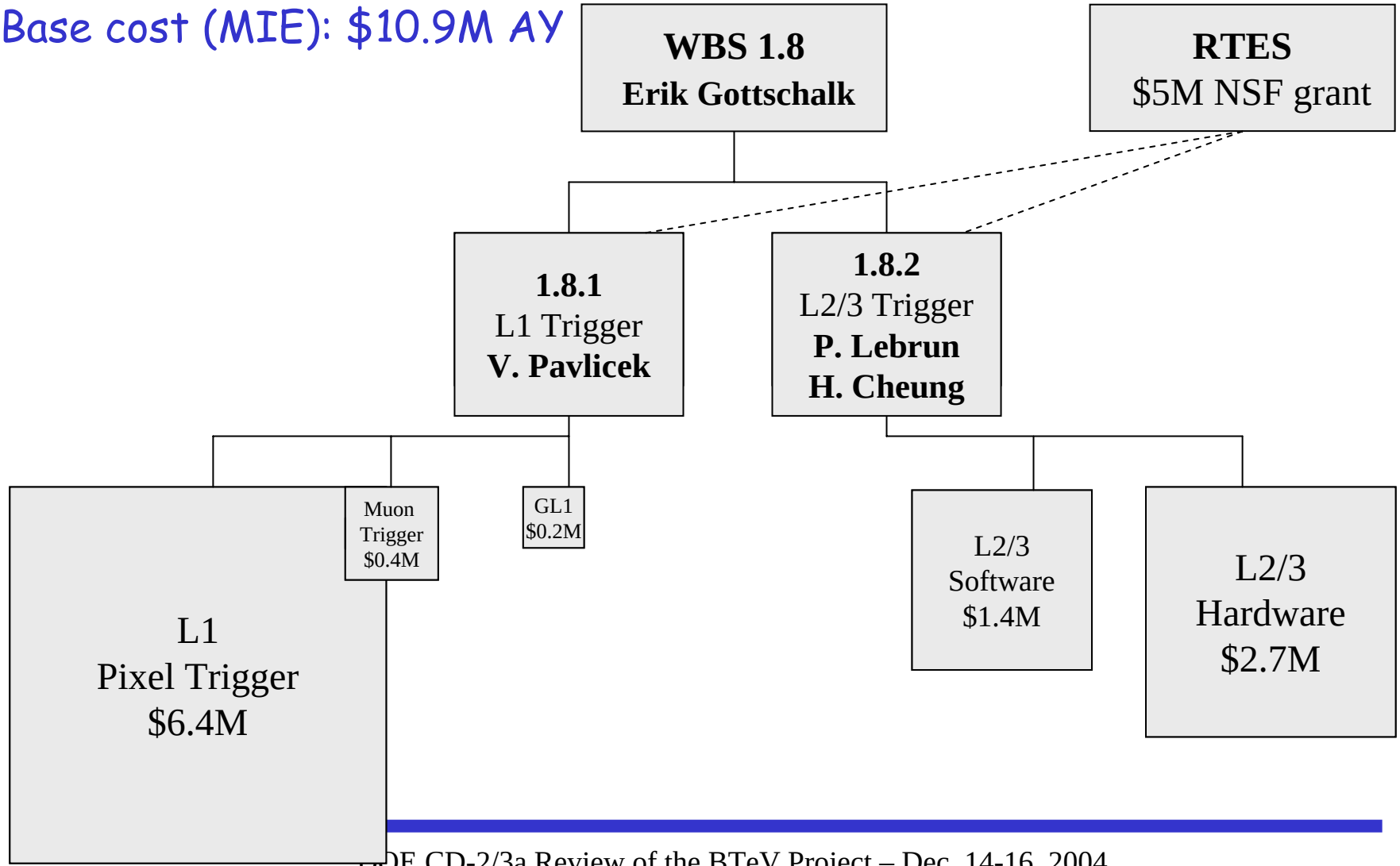
Base cost (FY05 dollars): $11.4M (Material: $7.8M, Labor: $3.6M)

Base cost (MIE): $10.9M AY



Base cost (FY05 dollars): $11.4M (Material: $7.8M, Labor: $3.6M)

Base cost (MIE): $10.9M AY



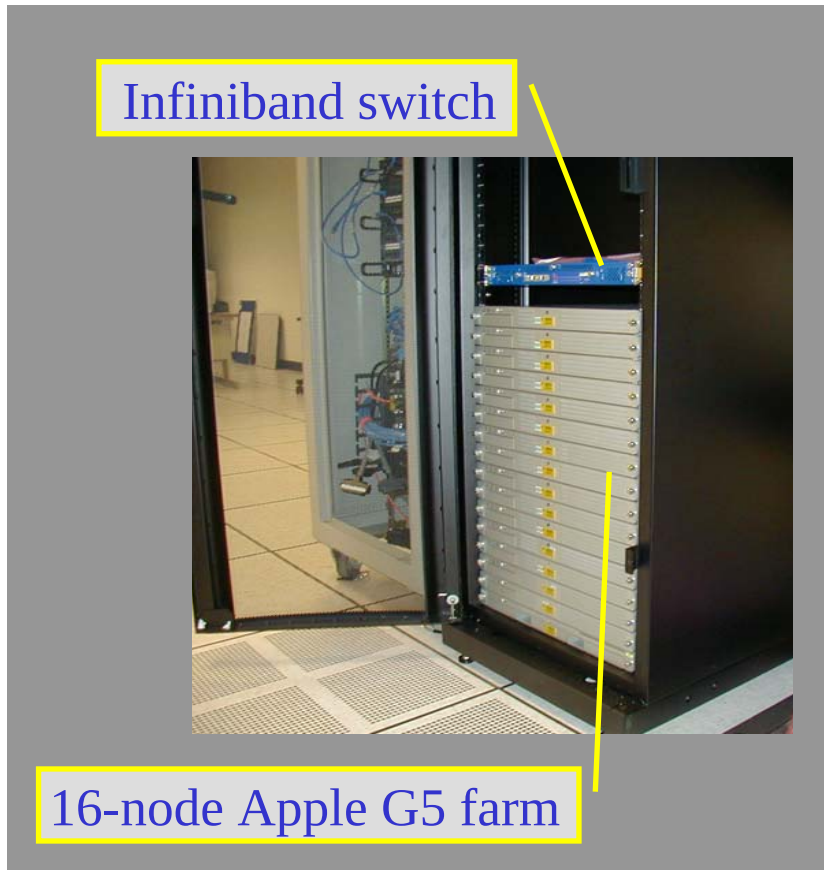
Trigger Development WBS 1.8

We have three phases of hardware development (pre-pilot, pilot, production), and two parallel stages of L2/3 software development beginning in FY05 and FY06, respectively.

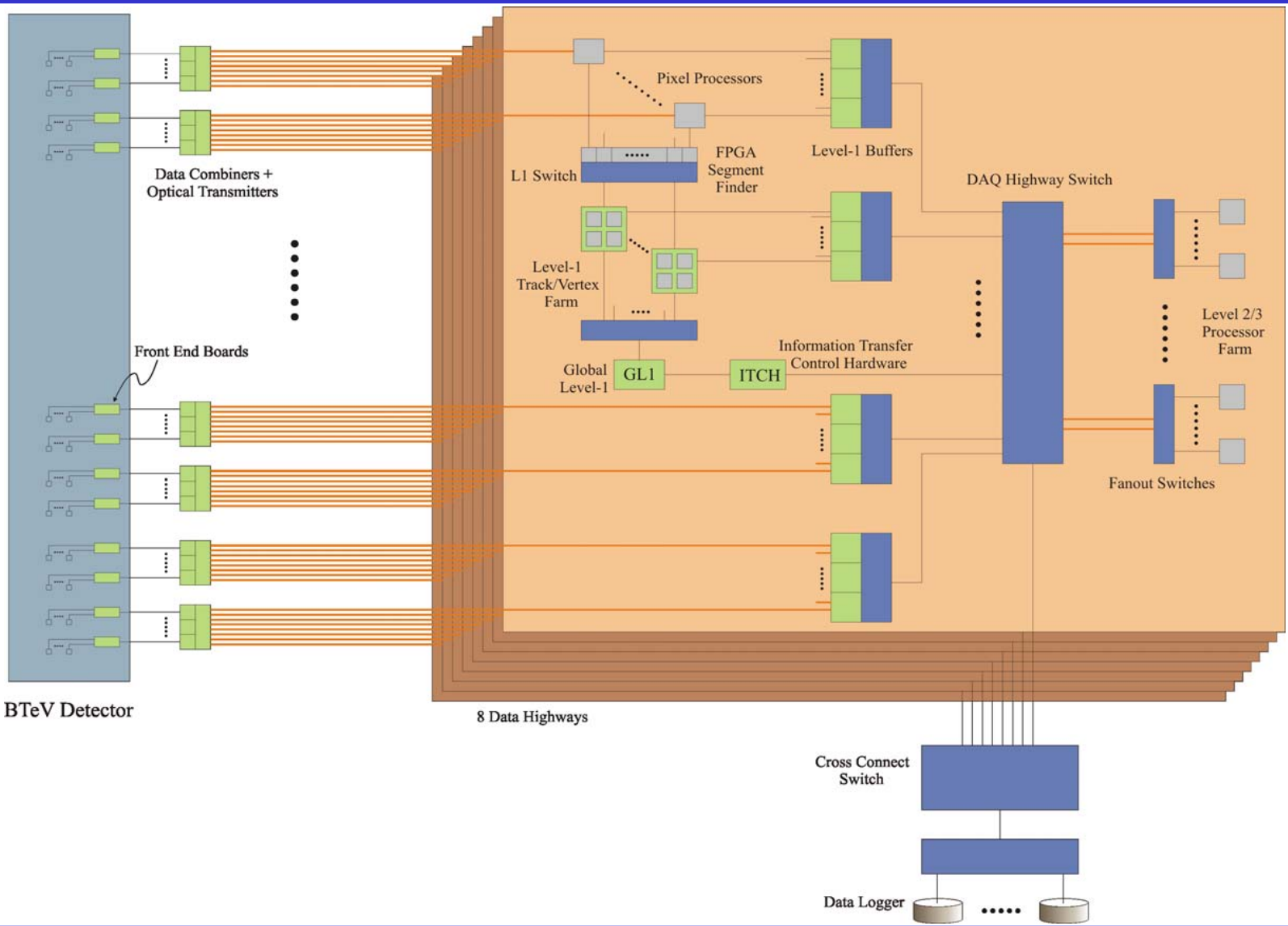
- L1 hardware and software (3-phase development)
  - Pre-pilot Switch & Farm (FY05) – hardware installation at FCC completed
  - Pilot (FY05 & FY06 with integration in FY07)
  - Production (begin 4-highway production in FY07)
- L2/3 hardware (3-phase development)
  - Pre-pilot (FY05 & FY06) – hardware installation at FCC completed
  - Pilot (5% in FY07)
  - Production (begin 4-highway production late in FY07)
- Stage 1 software – primarily L2 trigger code (development begins FY05)
  - L2 algorithm exists & satisfies efficiency, rejection, and timing requirements
  - Development effort is focused on detector alignment, framework, & utilities
- Stage 2 software – primarily L3 trigger code (development begins FY06)
  - L3 background rejection (factor of 2) is achievable with tracking detectors
  - Additional L3 algorithms are needed for online monitoring of data quality
  - L3 algorithms and online monitoring support BTeV physics analyses
  - L3 code development has scope contingency

Technical Progress Since CD-1 Review WBS 1.8

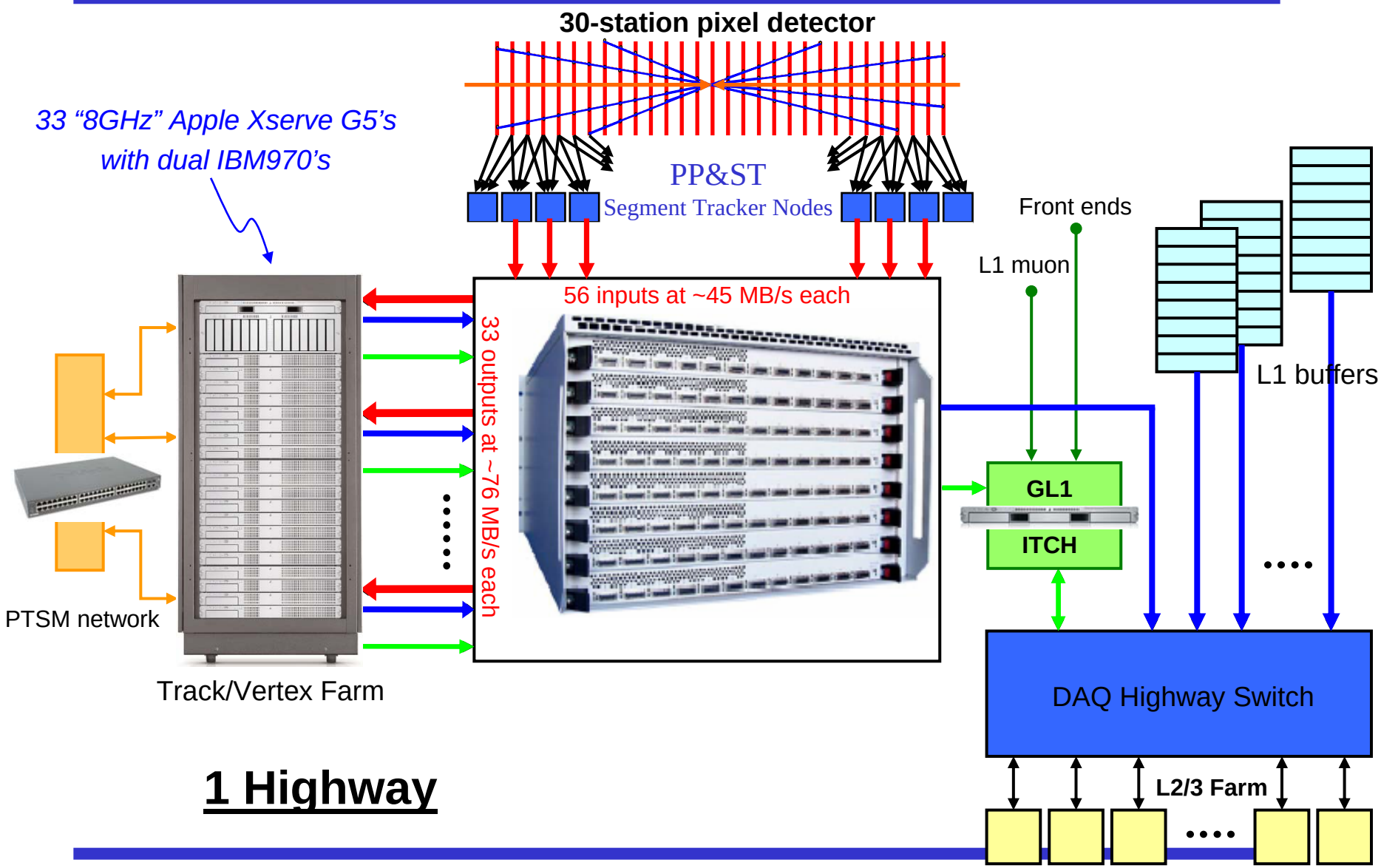
- Modified baseline architecture for L1, replacing two of three custom-designed trigger subsystems with commodity hardware. The revised WBS has "8 GHz" PowerPC processors (consistent with IBM roadmap) & Inifiniband switches.
  - Performed L1 network simulations
  - Reviewed results in the trigger group
  - Presented results to BTeV Tech. Board
  - PCR approved: August 2004
- Purchased and installed 16 Apple G5 (dual 2 GHz) nodes and an Infiniband switch at Feynman Computing Center
- Started evaluation of real-time operating systems for the L1 trigger
- Acquired and installed a 100-node pre-pilot farm for the L2/3 trigger (located next to the L1 hardware).



Three-level, eight-highway trigger/DAQ architecture

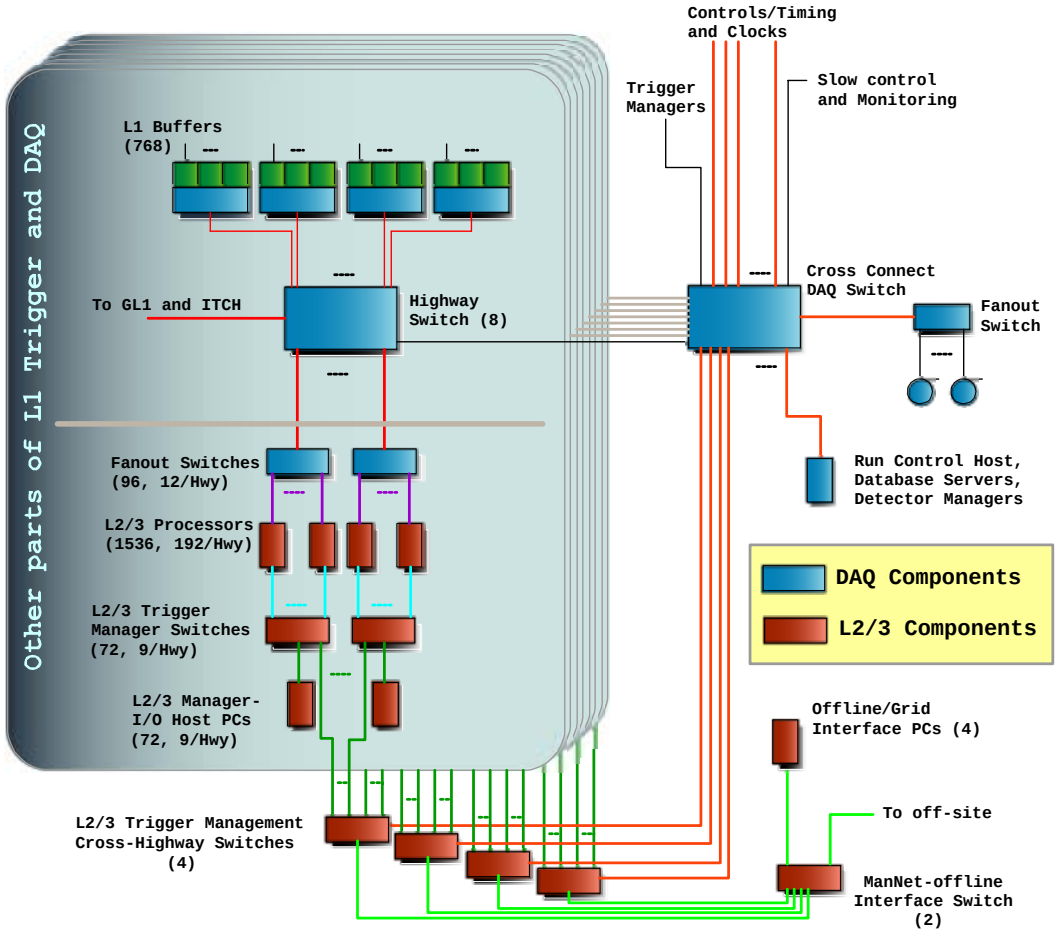


L1 Trigger Architecture (1 Highway) WBS 1.8



1 Highway

L2/3 Trigger Hardware WBS 1.8



Baseline Design

- L2/3 Processor farm consists of 1536 “12 GHz” CPUs (dual-CPU 1U rack-mount PCs)
- L2/3 trigger includes Manager-I/O Host PCs for database caches, worker management, monitoring, and event pool cache
- L2/3 Hardware in

L2 and L3 Trigger Software WBS 1.8

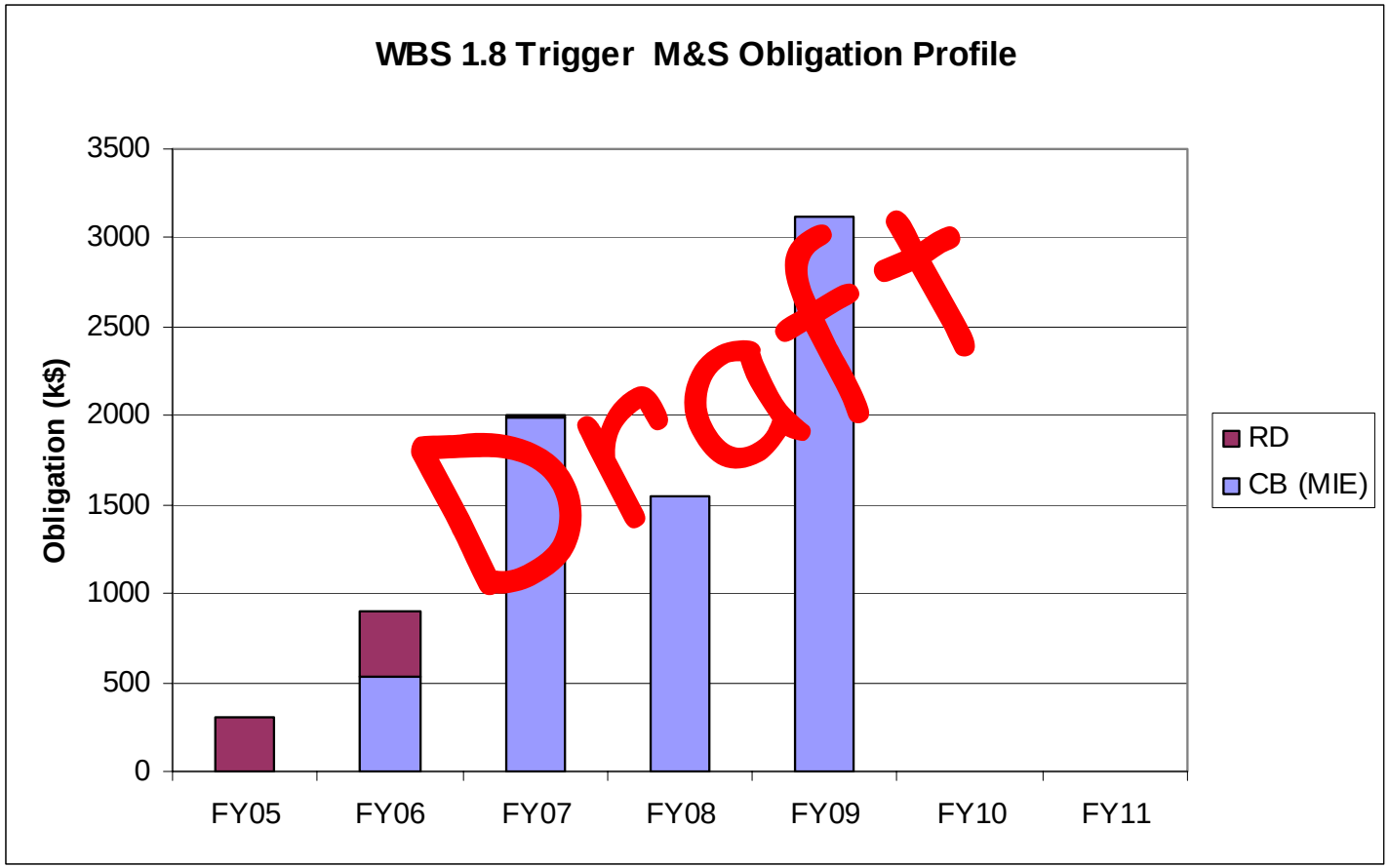
- L2 and L3 reconstruction software (tracks, vertices, photons, π^0's, hyperons, neutral kaons, particle identification)
- L2 and L3 trigger algorithms
- Global L2 and Global L3 software (trigger lists & selection criteria)
- Alignment and calibration software
- Monitoring, feedback and event display software
- Software framework, utilities, and interfaces to databases
- DAQ interface software
- Offline filter and fast charm/beauty monitoring software (high-level filtering and monitoring software)

Construction Cost WBS 1.8

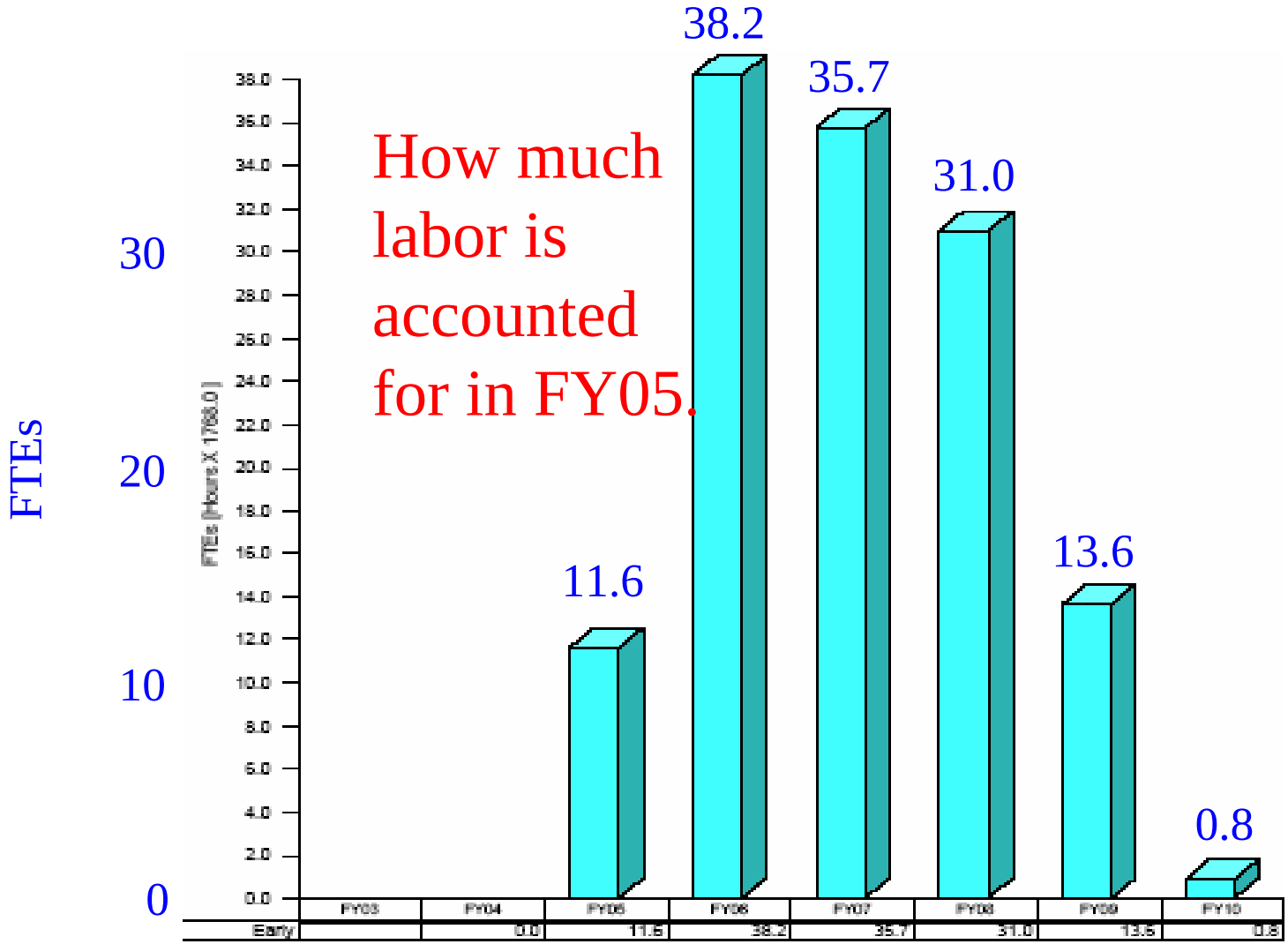
Activity ID	Activity Name	Base Cost ($)	Material Contingency (%)	Labor Contingency (%)	Total FY05	Total FY06	Total FY07	Total FY08	Total FY09	Total FY10	Total FY05-10
1.8.1	L1 Hardware & Software	6,769,409	37	38	607,014	263,1[illegible]	784,095	1,723,635	2,920,308	0	9,298,179
1.8.2	L2/L3 Hardware & Software	4,133,488	33	88	1[illegible]9,8[illegible]5	1,1[illegible]770	1,417,068	1,887,830	1,926,255	0	6,503,777
1.8.3	Trigger Electronics & SW Subproj Mgmt	230,199	16	24	46,879	54,336	53,697	53,697	53,484	19,178	281,271
1.8	file_18S_v10_091504	11,133,096	36	65	793,747	2,450,235	4,254,859	3,665,162	4,900,047	19,178	16,083,228

Draft

M&S Obligation Profile by Fiscal Year WBS 1.8

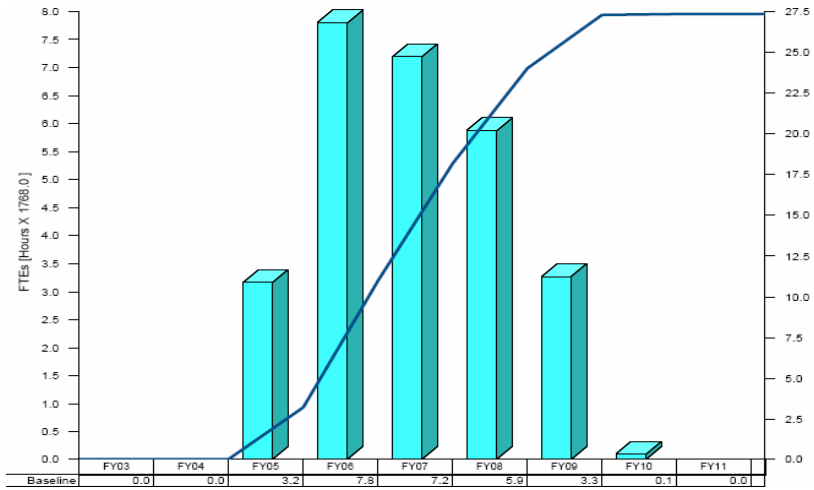


Labor Profile by Fiscal Year (Base Plan) WBS 1.8

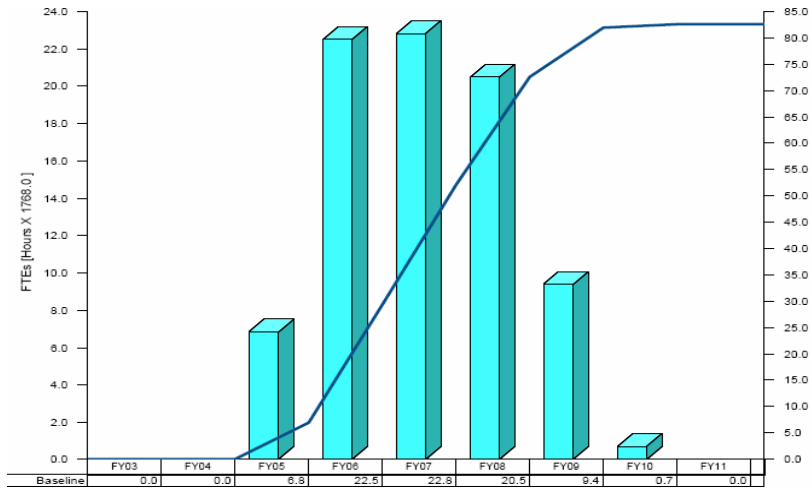


Labor Profiles by Fiscal Year (Base Plan) WBS 1.8

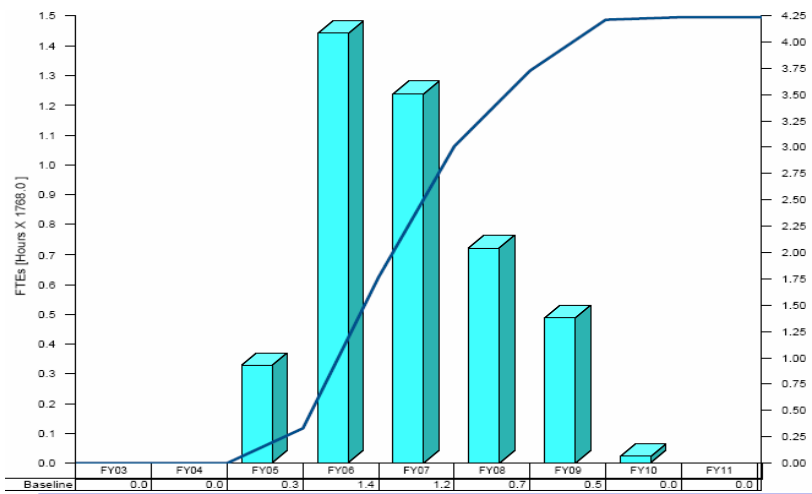
Technical Labor (Fermilab)



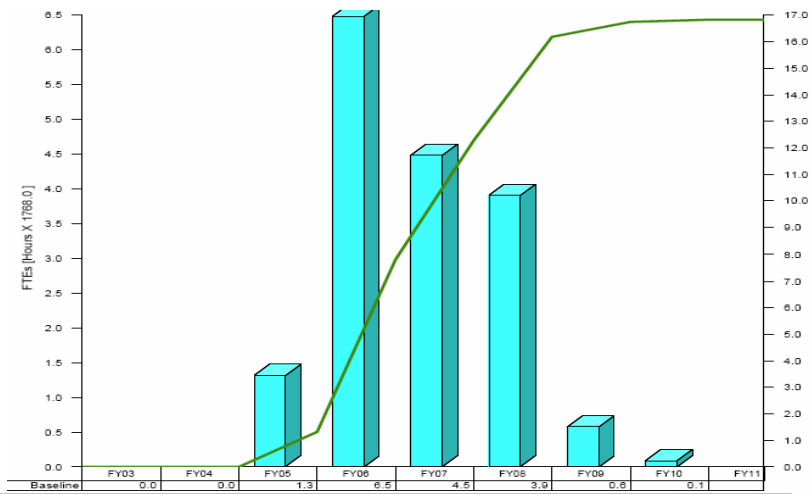
Physicist Labor (Fermilab)



Technical Labor (University)



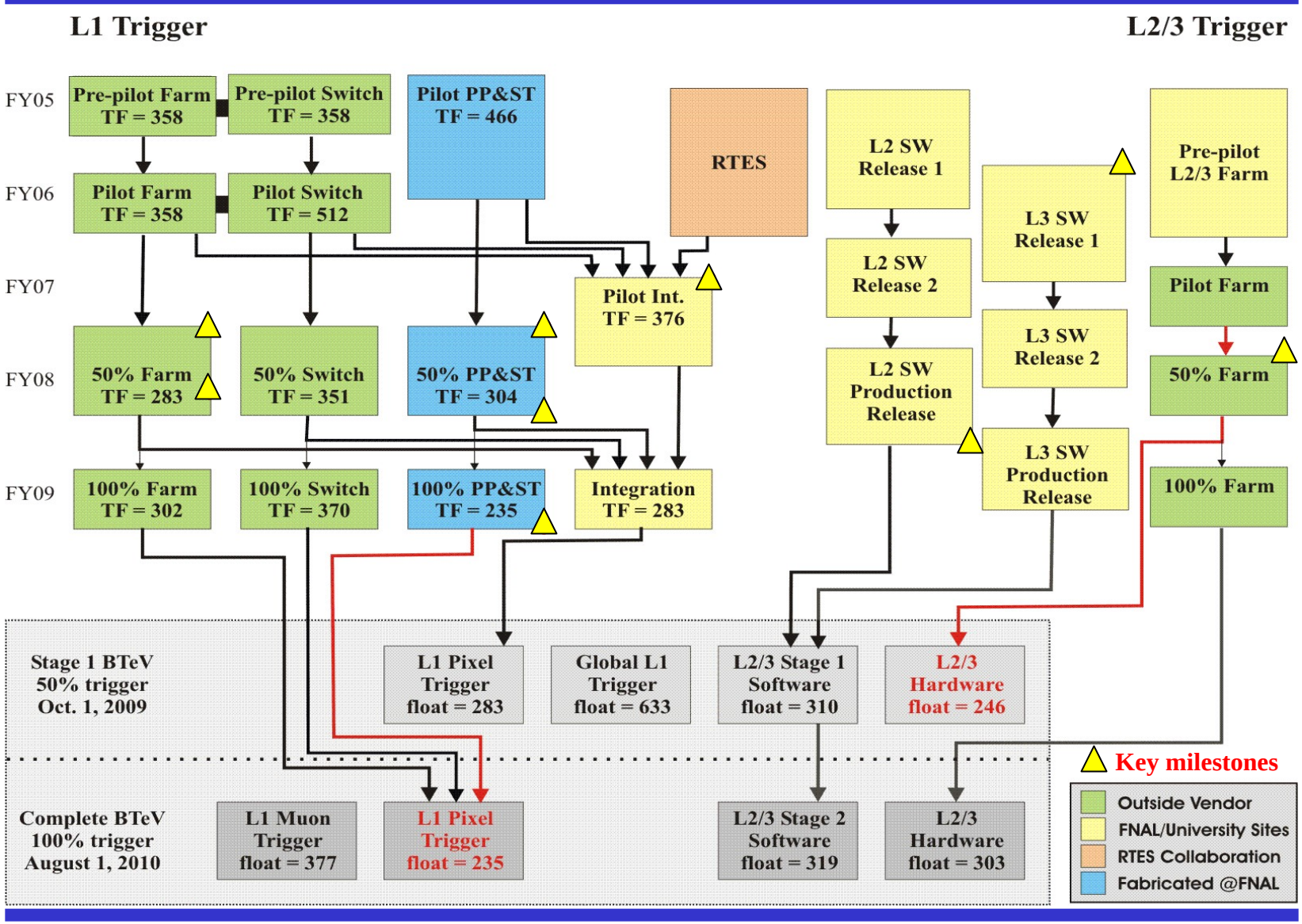
Physicist Labor (University)



- Multi-color labor plot (with table?)

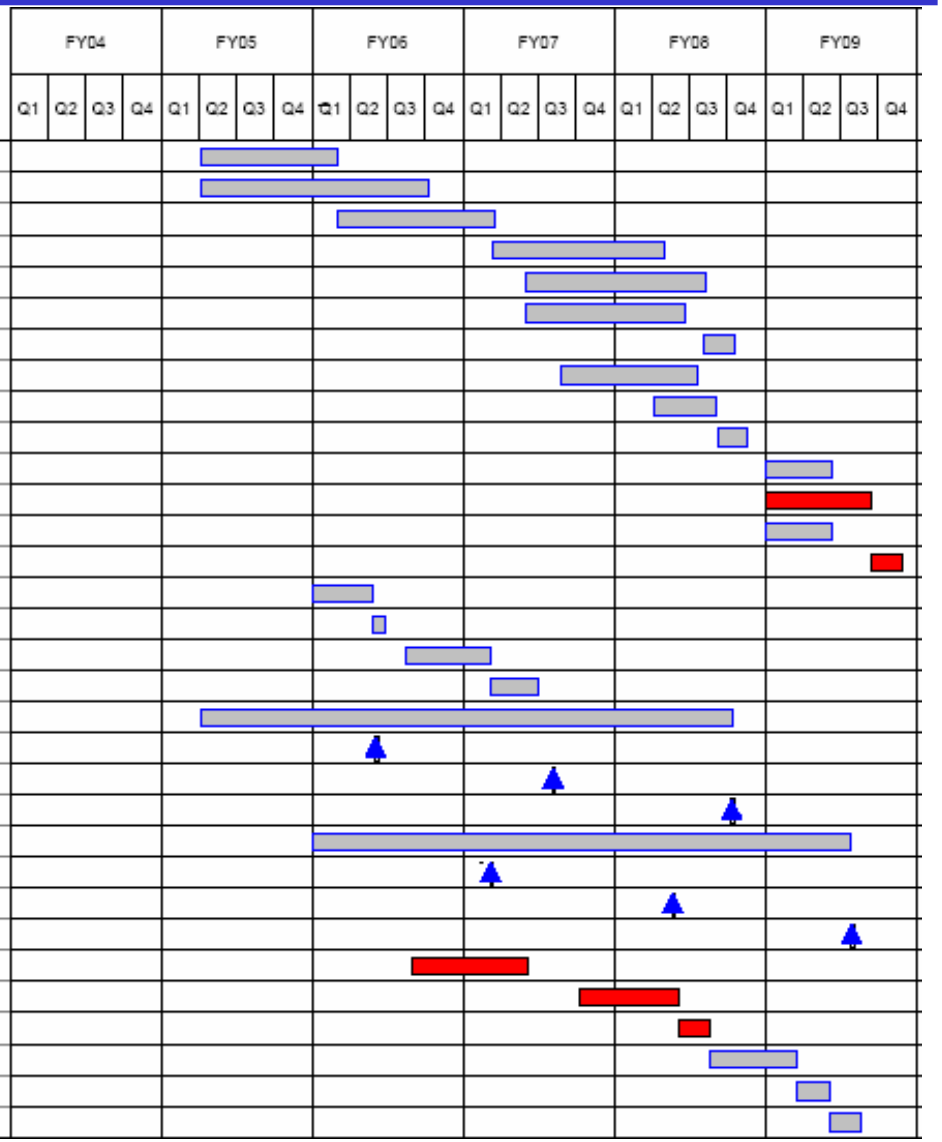
- Labor ramp up for FY06 (moving from 2.5 to 15 FTE)
- Fractional effort in FY05 (6 people 50% or less), move to full time
- New institutions including DAQ in MOU (Houston, Iowa) in addition to OSU. Working on MOUs now. DOE approval should attract more or expand existing participation.
- New hire posting in FY05 to work off project, starting on BTeV in FY06
- Ongoing discussions with FNAL/CD management in identifying interest and expertise for FY06 effort, and project assignments are being made appropriately (eg, database and networking area).
- FNAL/CD technical staff has expressed interest and is keeping eyes on the project at a low level (more work would be happening in FY05 if funding resources were available).

Project Flow (Base Plan) WBS 1.8



Gantt Chart (Base Plan) WBS 1.8

WBS	Activity Desc.
1.8.1.1.2.1	Pixel L1 Farm Prepilot P0
1.8.1.1.3.1	Preproc & SegTrk SubSys Pilot P1(I)
1.8.1.1.4.1	Pixel L1 Farm Pilot P1(f)
1.8.1.1.6	Pixel Trigger Pilot Integration=P1(Int)
1.8.1.1.8.1	Preproc & SegTrk SubSys Production P2.2
1.8.1.1.9.1	Pixel L1 Farm Production P2.2
1.8.1.1.10	Pixel Trigger 2-Hwy Integration=P2.2(Int)
1.8.1.1.12.1	Preproc & SegTrk SubSys Production P2.4
1.8.1.1.13.1	Pixel L1 Farm Production P2.4
1.8.1.1.14	Pixel Trigger Integration=P2.4(Int)
1.8.1.1.16.1	Pixel L1 Farm Production P2.6
1.8.1.1.17.1	Preproc & SegTrk SubSys Production P2.8
1.8.1.1.18.1	Pixel L1 Farm Production P2.8
1.8.1.1.19	Pixel Trigger Integration=P2.8(Int)
1.8.1.3.1	GL1 Trigger Pilot=GL1_P1
1.8.1.3.2	GL1 Trigger Pilot Integration=GL1_P1(Int)
1.8.1.3.3	GL1 Trigger Production=GL1Farm_P2
1.8.1.3.4	GL1 Trigger Production Integration=GL1_P2(Int)
1.8.2.2.1	L2/L3 SW Stage 1 Development
1.8.2.2.3	TSM: Done - Stage 1 Release 1
1.8.2.2.5	TSM: Done - Stage 1 Release 2
1.8.2.2.7	TSM: Done - Stage 1 Production Release
1.8.2.2.9	L2/L3 SW Stage 2 Development
1.8.2.2.11	TSM: Done - Stage 2 Release 1
1.8.2.2.13	TSM: Done - Stage 2 Release 2
1.8.2.2.15	TSM: Done - Stage 2 Production Release
1.8.2.3.1.4	build pilot workers and hosts System
1.8.2.3.1.5.2.1	Manuf & Del of Prod Farm worker HW 1st Ship
1.8.2.3.1.5.2.2	Manuf & Del of Prod Farm worker HW 2nd Ship
1.8.2.3.1.5.2.3	Manuf & Del of Prod Farm worker HW 3rd Ship
1.8.2.3.1.5.2.4	Manuf & Del of Prod Farm worker HW Last Ship
1.8.2.3.1.5.2.6.5	Int+Test whole L23 Farm Sys under C0 condit



Staged Trigger Components WBS 1.8

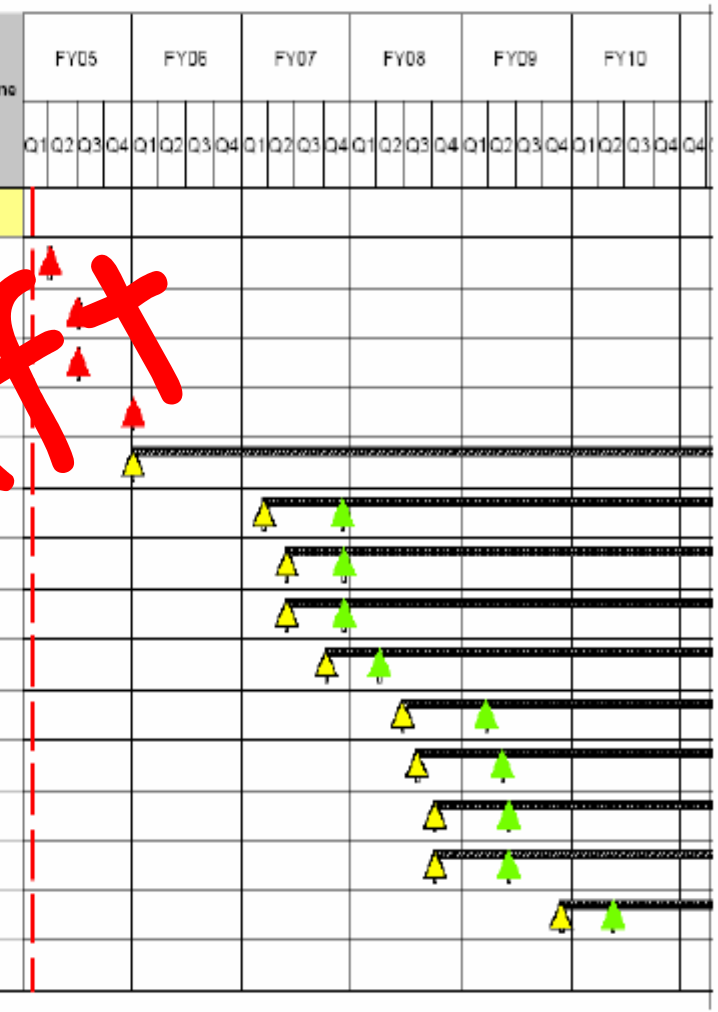
- Stage 1 BTeV Trigger – 50% trigger system
  - Need-by date: October 1, 2009
  - Ready by October, 2008 (12 months of float)
  - 50% of L1 pixel trigger hardware (100% of L1 software)
  - 100% of Global Level 1 (GL1) hardware and software
  - 50% of L2/3 trigger hardware
  - Final production release of Stage 1 software (primarily L2 code)
  - Second production release of Stage 2 software (primarily L3 code)
- Stage 2 BTeV Trigger – 100% trigger system
  - Need-by date: August 1, 2010
  - Ready by September, 2009 (11 months of float)
  - Remaining 50% of L1 and L2/3 trigger hardware
  - 100% of L1 muon trigger
  - Final production release of Stage 2 software

Critical Path Analysis WBS 1.8

- Stage 1 BTeV trigger (246 workdays of float)
  - Completing the first four highways for the L2/3 trigger has the lowest total float for the **Stage 1 BTeV detector**, with 246 days of float. The activities involve the procurement of computer farms. Procurement is delayed to obtain more processing capabilities for lower cost. The procurement of processors for the L2/3 trigger has minimal schedule risk, and there is considerable expertise for this work at Fermilab.
- Stage 2 BTeV trigger (235 workdays of float)
  - The completion of the remaining four highways of the L1 pixel preprocessor and segment tracker (PP&ST) hardware has the lowest total float for the **Stage 2 BTeV detector**, with 235 days of float. By the time this work is started we will have considerable expertise building, testing, and commissioning PP&ST hardware. Therefore, we expect minimal schedule risk, since four trigger highways will be fully operational by the time this work begins.

Key Milestones WBS 1.8

Activity ID	Activity Desc.	Milestone Tier (C4)	Early Start	PMB Baseline Date
1.8 -- Trigger Electronics and Software				
1.8.4.2.1.2	T0M: CD-1 Approve Preliminary Baseline Range	T0	30Dec2004	30Dec2004
1.8.4.2.1.3	T0M: CD-2 Approve Performance Baseline	T0	31Mar2005	31Mar2005
1.8.4.2.1.4	T0M: CD-3a Approve Limited Construction	T0	31Mar2005	31Mar2005
1.8.4.2.1.5	T0M: CD-3b Approve Start of Construction	T0	30Sep2005	[illegible]2005
1.8.4.2.4.0	T3M: Start L3 software development	T3	03[illegible]005	03Oct[illegible]
1.8.4.2.3.1	T2M: Trigger pilot system ready for testing		[illegible]Dec2006	[illegible]007
1.8.4.2.4.1	T3M: Start L1 2-hgwy pixel proc/seg trkr prod	T3	0[illegible]r2007	04Sep2007
1.8.4.2.4.3	T3M: Start L1 2-highway farm production	T3	01Mar2007	04Sep2007
1.8.4.2.4.6	T3M: Start L2/L3 farm worker node procurement	T3	09Jul2007	02Jan2008
1.8.4.2.4.4	T3M: End L1 2-highway farm production	T3	18Mar2008	16Dec2008
1.8.4.2.4.2	T3M: End L1 2-hgwy pixel proc/seg trkr prod	T3	06May2008	10Feb2009
1.8.4.2.3.2	T2M: 1st prod release: Lvl 2/3 Trig software	T2	10Jul2008	02Mar2009
1.8.4.2.4.7	T3M: 1st prod release: Lvl 2/3 Trig software	T3	10Jul2008	02Mar2009
1.8.4.2.4.8	T3M: Trig sys & integration with DAQ complete	T3	24Aug2009	18Feb2010
1.8.4.2.1.6	T0M: CD-4 Approve Start of Ops - Project Closeout	T0	30Jun2011	30Jun2011



Draft

Risk Analysis WBS 1.8

WBS Item	Risk Event	Response/Mitigation Strategy
For example: 1.8.1.1.2.1, 1.8.1.1.4.1	Baseline processor fails to meet requirements	Benchmark and qualify more than one processor during R&D or early construction phase. Have a 2nd option ready if the 1st option is unsatisfactory.
For example: 1.8.1.1.8.1.1.1, 1.8.1.2.1.2	Pixel segment tracker or muon preprocessor algorithm exceeds the size of the selected FPGA. Larger FPGA increases the cost	Use contingency funds to upgrade to a bigger and more expensive FPGA. Consider other implementation alternatives early in the design stage. Consider simplifying the algorithms.
For example: 1.8.1.1.3.1.1.1, 1.8.1.1.8.1.1.1	Communication links do not satisfy error rate specifications	Use contingency to modify PC boards, buy new parts, connectors, or cables.
For example: 1.8.1.1.4.1.1.5, 1.8.2.2	Shortage of software developers	Prioritize critical tasks. Use contingency to hire software developers.
Numerous WBS items	Experienced people leave the trigger project.	Be sure that more than one person is working on critical tasks. Use contingency funds to hire the person who leaves as a temporary consultant, and transfer their expertise to existing or new personnel.

Response to CD-1 Recommendations WBS 1.8

- Develop a schedule which (a) completes critical design and validation activities as soon as possible and is ready for production six to nine months in advance of the production start date, and (b) completes production of the trigger and data acquisition systems six to nine months in advance of first collisions.
  - (a) Critical design and validation activities have been an ongoing effort. We will complete the L1 PP&ST system 8 months before the start of production.
  - (b) We have developed a schedule that completes 50% of the L1 trigger more than 13 months before the need-by date for the Stage 1 detector, and completes 50% of the L2/3 trigger almost one year before the need-by date.
- Re-evaluate the basis of estimate of the FPGA costs to allow for uncertainty in the de-escalation profile.
  - We no longer de-escalate FPGA costs.
- Quickly identify and apply new individuals and groups to provide the physicist effort for by the WBS.
  - We have identified new individuals and groups (Univ. of Houston, Southern Methodist University, Univ. of Virginia), and are continuing to do so.

FY05 Plan WBS 1.8

- L1 Pixel Preprocessor & Segment Tracker (PP&ST) Pilot – (RD)
  - Develop specifications for the PP&ST subsystem
  - Design, simulate, and develop firmware for Pilot PP&ST trigger highway
- L1 Trigger Pre-pilot Switch and Farm – (RD & PED)
  - Purchase & install 16-node Apple G5 Pre-pilot Farm
  - Evaluate real-time operating system software for L1 Farm
  - Continue development of L1 trigger algorithm & L1 software framework
  - Purchase additional hardware for Pre-pilot engineering design effort
- L2/3 Trigger Software – (RD & PED)
  - Develop L2 trigger methods and evaluate L2 trigger algorithms
  - Develop L2 trigger pre-production software
  - Develop Global L2 pre-production software
  - Develop L2 specifications (framework, alignment, calibration, utilities)

Conclusion

- Our team has a history of taking on difficult problems and solving them. Over time this has helped us develop the technical expertise that is needed to build the BTeV trigger.
- Examples of some of our achievements:
  - Developed a detached L1 vertex trigger for B physics in a hadron collider
  - Influenced pixel detector design by developing new L1 trigger algorithms (2-plane algorithm, “inner” & “outer” tracking, “exterior” hit elimination)
  - Implemented the L1 pattern recognition algorithm in FPGA hardware
  - Designed and built a multi-processor DSP prototype system
  - Developed expertise in low-level assembly language programming (DSPs)
  - Introduced concept of “highways” to simplify the trigger/DAQ architecture
  - Developed L2 algorithm that meets efficiency, rejection, timing requirements
  - Introduced commodity hardware as a replacement for DSP processing farm
- We are ready to move from prototype to system development, and have started to assemble a pre-pilot trigger highway for L1 and L2/3.

- Our cost and schedule for the development and construction of the BTeV trigger is robust and achievable, and has benefited from the feedback that we have received from past reviews.

Additional Presentations for WBS 1.8

More information on the BTeV trigger is available in these presentations:

WBS 1.8

- L1 pixel trigger – Vince Pavlicek
- L1 muon trigger – Mike Haney
- Global Level 1 – Vince Pavlicek
- L2/3 software – Paul Lebrun
- L2/3 hardware – Harry Cheung

Additional Slides

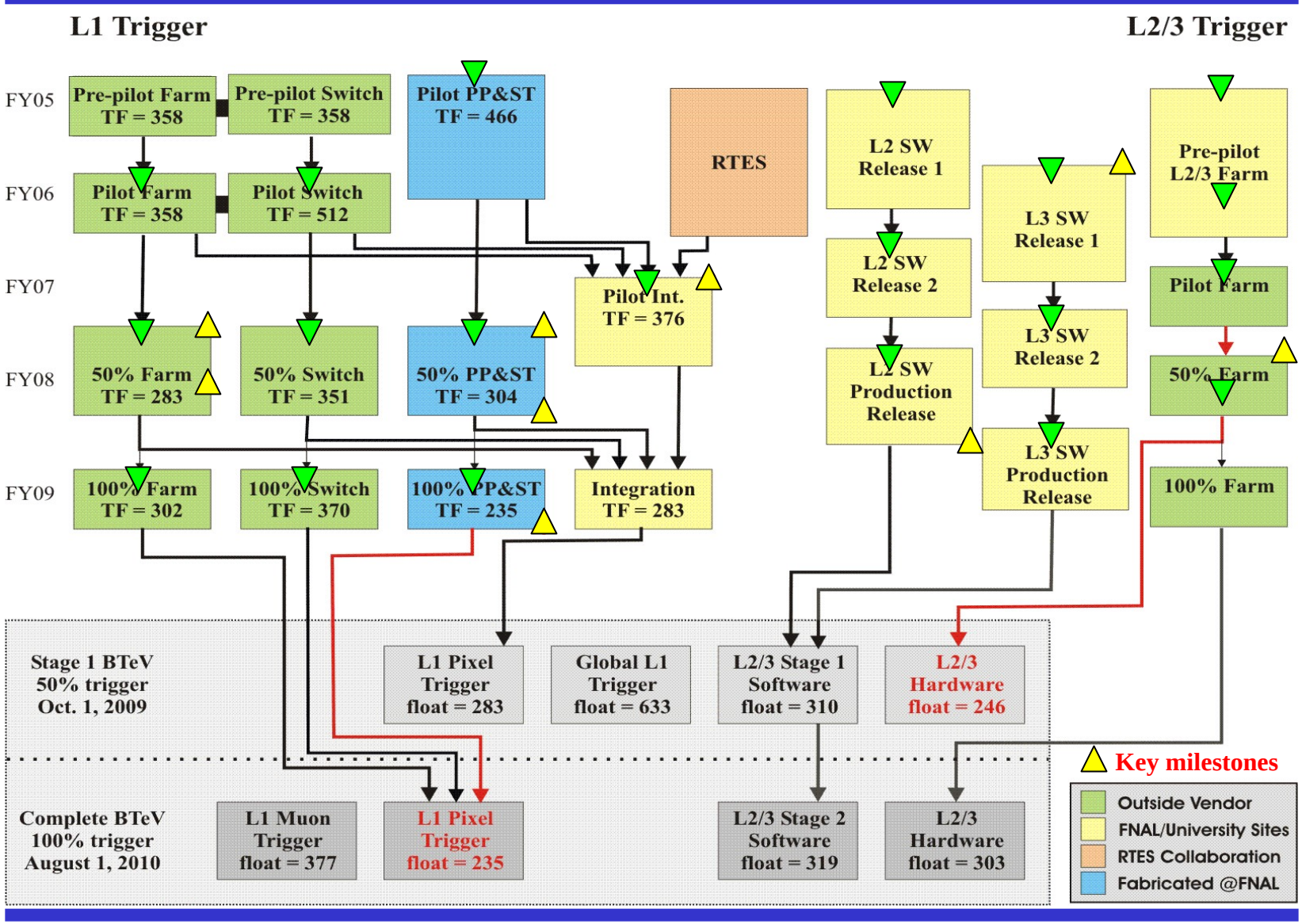
Trigger/DAQ Glossary

DB	Database
DCB	Data Combiner Board
DDR	Double Data Rate
DRAM	Dynamic Random Access Memory
FCC	Feynman Computing Center
FPGA	Field Programmable Gate Array
GBE	Gigabit Ethernet
GL1	Global Level 1
Infiniband	Third generation high-speed networking standard
ITCH	Information Transfer Control Hardware
L1B	Level 1 Buffer
PCI	Peripheral Component Interface
PCI-Express	High-speed serial version of PCI
PP&ST	Pixel Preprocessor and Segment Tracker
PTSM	Pixel Trigger Supervisor and Monitor
RCS	Run Control System
RTES	Real-Time Embedded Systems
SODIMM	Small Outline Dual Inline Memory Module
Xserve G5	Apple's PowerPC based 1U server with dual 64-bit processors

Base Plan Key Milestones WBS 1.8

T2	Trigger pilot system tested	Jan-07
T2,T3	Stage 1 production release of L2/3 software	Jul-08
T3	Begin L1 2-highway pixel processor & segment tracker production	Mar-07
T3	End L1 2-highway pixel processor & segment tracker production	May-08
T3	Begin L1 2-highway farm production	Mar-07
T3	End L1 2-highway farm production	Mar-08
T3	Begin L2/3 farm worker node procurement	Jul-07
T3	Begin L3 software development	Oct-05
T3	Complete trigger system and integration with DAQ	Aug-09

PMB Key Milestones WBS 1.8

T2	Trigger pilot system tested	Jul-07
T2,T3	Stage 1 production release of L2/3 software	Mar-09
T3	Begin L1 2-highway pixel processor & segment tracker production	Jul-07
T3	End L1 2-highway pixel processor & segment tracker production	Dec-08
T3	Begin L1 2-highway farm production	Jul-07
T3	End L1 2-highway farm production	Oct-08
T3	Begin L2/3 farm worker node procurement	Jan-08
T3	Begin L3 software development	Oct-05
T3	Complete trigger system and integration with DAQ	Feb-10

Project Flow (with SC tasks) WBS 1.8