



FPIX2, the BTeV pixel readout chip

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Abstract

A radiation tolerant pixel readout chip, FPIX2, has been developed at Fermilab for use by BTeV. Some of the requirements of the BTeV pixel readout chip are reviewed and contrasted with requirements for similar devices in LHC experiments. A description of the FPIX2 is given, and results of initial tests of its performance are presented, as is a summary of measurements planned for the coming year. © 2003 Elsevier Science. All rights reserved

Silicon pixel detector readout

1. Introduction

The most striking feature of BTeV, a dedicated b physics experiment now expected to start running in 2009 in the new CZero interaction region of the Fermilab Tevatron, is that the experiment will use data from a pixel vertex detector to reconstruct tracks and vertices *for every beam crossing*. The lowest level trigger will be an impact parameter trigger designed to identify events containing reconstructable decays of charm and bottom particles[1]. An R&D

program to develop a pixel readout chip for Tevatron experiments was started at Fermilab in 1997, and is now nearing completion.

2. Requirements

Since the edges of the BTeV pixel detector closest to the colliding beams of the Tevatron are expected to be exposed to approximately 3 Mrad per year of ionizing radiation ($\sim 10^{14}$ 1-MeV neutrons equivalent per year), the pixel readout chip must be extremely radiation tolerant and insensitive to single event

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effects. It must also be able to tolerate large sensor leakage current.

The chip must be optimized for the beam crossing structure of the Tevatron. Currently, this means a time between crossings of 396 ns. At the time this chip design was initiated, the Fermilab long range plan called for reducing the time between crossings to 132 ns, so the chip has been designed assuming that the time between crossings might be as small as 132 ns or as large as 396 ns.

Finally, since the trigger requires all pixel information from every crossing, the readout chip must have a very high-speed zero-suppressed readout. At the BTeV design luminosity, the rate of proton-antiproton interactions is approximately 15 MHz. The BTeV pixel readout chip has been designed with enough output bandwidth to insure that essentially no data is lost due to readout deadtime at the design luminosity, and that the data loss at three times the design luminosity is also minimal.

The radiation hardness and leakage current requirements of BTeV are essentially the same as for the LHC experiments ATLAS and CMS. The longer time between crossings (132, or even 396 ns, compared with 25 ns) means that discriminator timewalk is *much* less of a problem for FPIX2 than for the LHC pixel readout chips. The readout requirement is also very different. BTeV pixel chips located near the colliding beams require *much* greater output bandwidth than is required of the LHC pixel chips. On the other hand, the BTeV readout chip is not required to store data on-chip during the relatively long time required to make a trigger decision. This means that the BTeV chip can hold hit data awaiting readout in the pixel cells, rather than in memory located in the chip periphery, without incurring unacceptable pixel deadtime and associated loss of efficiency.

3. FPIX2 Description

3.1. Overview

A block diagram of the FPIX2 pixel readout chip is given in Fig. 1 and a picture of the layout is shown

in Fig. 2. The chip was produced by the Taiwan Semiconductor Manufacturing Company using its 0.25 μ CMOS process. The design of this chip started in 1998 and uses radiation tolerant layout procedures. The initial design allowed the chip to be implemented either in the TSMC 0.25 μ CMOS process, or in the IBM 0.25 μ CMOS process[2]. The final design has been optimized for TSMC.

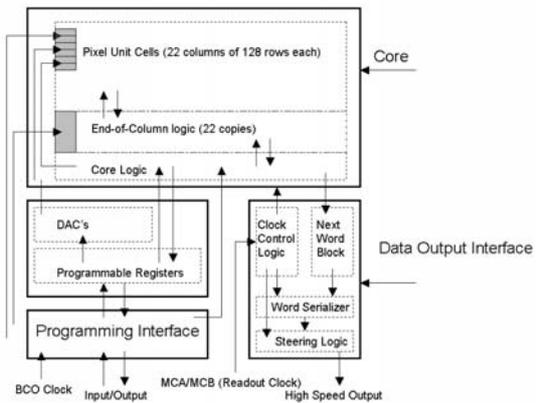


Fig. 1. FPIX2 block diagram

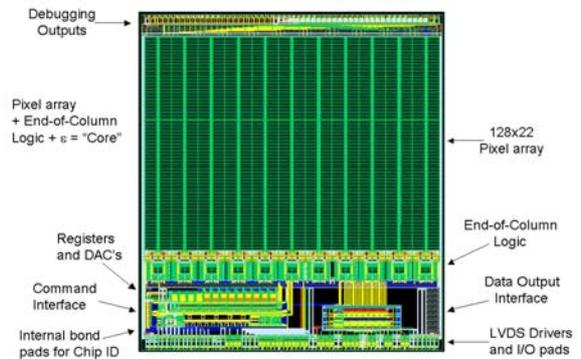


Fig. 2. FPIX2 layout.

The basic design was verified by a series of small test chips. Exposures of these chips to gammas from ^{60}Co and to 200 MeV protons at the Indiana University Cyclotron Facility have demonstrated that the analog circuits suffer no degradation in performance up to a total dose of 87 Mrad, with only minor changes required to bias conditions. The digital cells are insensitive to total dose at this level of exposure. No latch-up or evidence of gate rupture

has been observed. Single event upset cross sections have been measured using the 200 MeV proton beam and are typically less than 10^{-15} cm² per bit[3].

3.2. Pixel Unit-cell

The FPIX2 pixel unit-cell consists of a continuous-time-filter amplifier, eight comparators which together form a 3-bit flash ADC, and digital logic. The digital circuitry encodes the ADC information, stores the hit information until an “output data” command is received from the end-of-column logic, and transmits the hit data to the data-output interface. A block diagram of the pixel unit-cell is given in Fig. 3, and a picture of the layout of four 50μ x 400μ pixels is shown in Fig. 4.

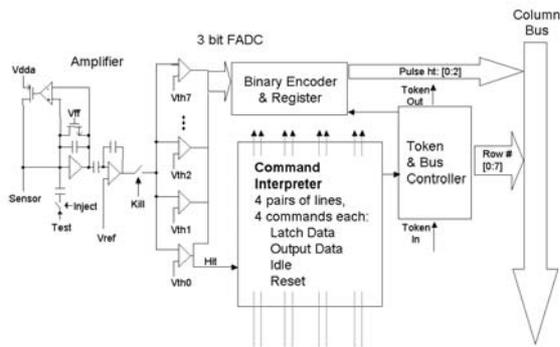


Fig. 3: FPIX2 pixel unit-cell.

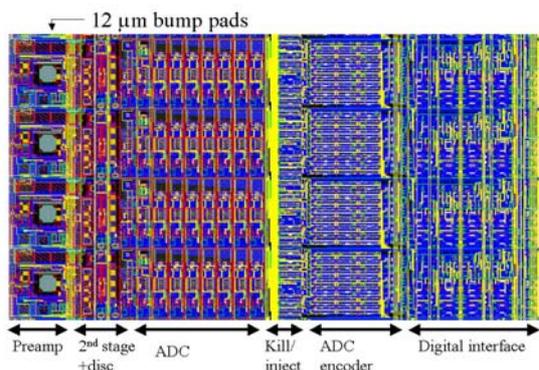


Fig. 4: Layout of four FPIX2 pixel unit-cells.

3.3. FPIX2 Readout

Data is driven from a hit pixel unit-cell onto the “core output-bus,” which is 23 bits wide. The data word consists of information generated in the pixel unit-cell (7-bit row number and 3-bit ADC value), plus a 5-bit column number and an 8-bit time-stamp (“BCO number”), which are added by the end-of-column logic. The data output interface latches data from the core output bus, serializes the data, and drives it off chip. The FPIX2 readout architecture and normal operation are described in detail in [4].

The output data format is shown in Fig. 5. Data words are distinguished by the fact that bits 1-13 are never allowed to all be zero. In order to ensure that a data word cannot have zeros in all of these bits, the 22 column numbers are encoded in five bits using numbers which do not have zeros in both of the low order binary places. Synchronization between the FPIX2 and the “pixel data combiner board,” which receives the output data, is established and maintained using a “sync/status” word. Whenever data is unavailable for output, the FPIX2 transmits the sync/status word. Data is read out of the FPIX2 column-by-column in a round-robin fashion. At least two sync/status words are output each time the token controlling which column is read out passes through all 22 columns. The data combiner board also verifies synchronization as it receives each data word by checking that bit 0 is “1.”

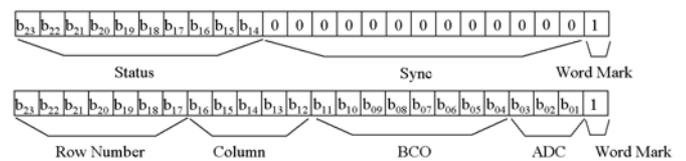


Fig. 5: FPIX2 output data format.

Data is output from FPIX2 using Low Voltage Differential Signaling (LVDS). The FPIX2 output consists of a clock, and a programmable number (1, 2, 4, or 6) of LVDS data pairs. FPIX2 chips located close to the beam will be configured to use 6 output pairs. Those located farther away from the beam will be configured to use fewer output pairs. Most chips in the system will use only one output pair. Both the

data output clock and the readout clocks used internally by the FPIX2 are derived from a pair of nominally 70 MHz clocks supplied to the FPIX2 by the data combiner board. Data is latched by the data combiner board at both edges of the data output clock; so the link speed is 140 Mbps per data pair.

The frequency of the internal readout clock used in the FPIX2 is not the same for all chips in the system, but depends on the number of serial data links being used for output data (see Table 1). The frequency of the internal readout clock is the data transfer bit rate divided by the ratio of the word size of 24 bits to the number of active output data links. This relationship between the internal readout clock frequency and the number of data links being used ensures that the time required to drive a data word off chip is equal to the readout clock period. This means that no buffer memory is required in the data output interface.

Table 1: FPIX2 internal readout clock frequency, assuming each data link operates at 140 Mbps.

Configuration	Readout Clock Frequency
6 output pairs	35 MHz
4 output pairs	23.3 MHz
2 output pairs	11.7 MHz
1 output pair	5.8 MHz

4. Bench-test results

Three versions of the FPIX2 have been fabricated by TSMC, all with the same digital logic, but with three different versions of the analog cells:

- Version A is unchanged from the earlier test chips.
- Version B contains the same preamplifier as version A, but the second amplifier stage and the discriminator have been optimized for the TSMC process.
- Version C contains a higher gain preamplifier, which is optimized for TSMC. It also contains a unity-gain buffer between the first and second

amplifier stages, and the modified second stage and discriminator as in version B.

In initial bench tests (unbonded to pixel sensors), version A works as on earlier test chips. Version B and C work almost as expected, except for some oscillation problems when biased at nominal conditions. The origin of these problems are still under investigation. A readout bandwidth of more than 840 Mbps (6 output pairs) has been achieved. No crosstalk between output pairs is observed, and the analog performance is independent of the number of output pairs used.

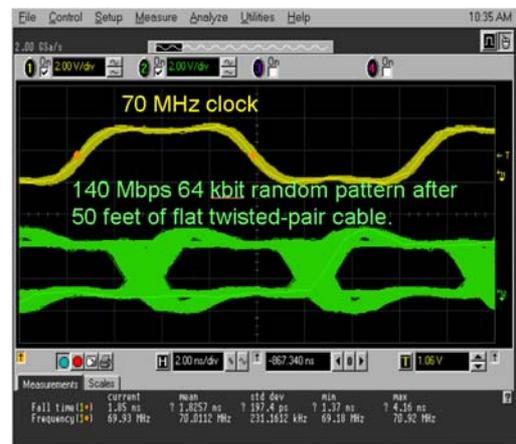


Fig 6: “Eye pattern” demonstrates that the FPIX2 nominal output bandwidth of 140 Mbps will not result in data loss due to the signal degradation after transmission over 50 feet of cable.

Fig. 6 shows the data output “eye pattern” measured using a test chip containing the final version of the FPIX2 data output interface. For this test, a 64000-bit long random pattern of ones and zeros was generated. This pattern was input to the data output interface and driven over a 50 foot long 100Ω flat twisted-pair cable. The more-than-5ns open “eye” demonstrates that the bit error rate at 140 Mbps should be negligible, and that it is not necessary to encode the pixel data to ensure that the differential pairs will be DC-balanced.

Measurements of amplifier noise and discriminator threshold dispersion are summarized in Table 2. The smaller threshold dispersion of version B with respect to version A reflects the optimization

of the discriminator design. The difference between version B and version C reflects the fact that version C has a larger preamplifier gain (and smaller dynamic range) than versions A or B.

Table 2: Amplifier noise and discriminator threshold dispersion measured on unbonded FPIX2 chips.

Version	Noise in e^-	Threshold Dispersion in e^-
A	70	231
B	70	176
C	59	125

The discriminator timewalk for 500 e^- overdrive is measured to be 122 ns for version A, and 103 ns for version C. This is the difference between the time delay between the injection of a very large pulse and the time that the discriminator fires, and the delay associated with an injected pulse that is only 500 e^- above the discriminator threshold.

5. Plans for the next year

Silicon pixel sensors designed to be read out by the FPIX2 have been produced by TESLA³ using the “moderated p-spray” technology developed for ATLAS[5]. These wafers (see Fig. 7) contain all of the module types required by the baseline BTeV pixel detector design, as well as a number of “single-chip” sensors and smaller test structures. A large number of these sensors will be bump bonded to FPIX2 readout chips. Hybrids will be assembled by VTT⁴ using solder bumps, and by AIT⁵ using indium bumps. We expect to receive the first hybrids at Fermilab before the end of 2003.

During the next year, bench tests will be carried out using hybrid assemblies, both before and after irradiation by 200 MeV protons. Hybrid assemblies

will also be tested as tracking devices in the newly configured 120 GeV “Meson test beam” at Fermilab⁶.

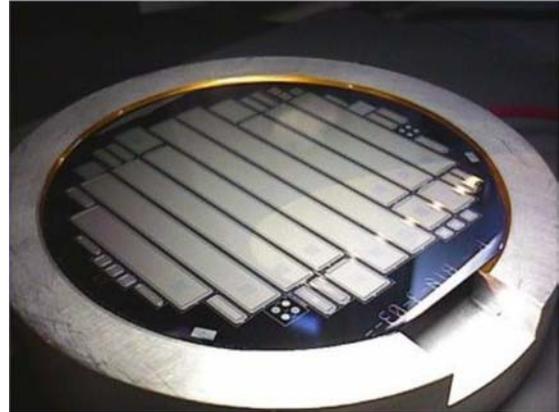


Fig. 7: BTeV p-spray sensor wafer

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³ TESLA Sezam, a.s., Roznov pod Radhostem, The Czech Republic (see <http://www.onsemi.cz>).

⁴ VTT Technical Research Center of Finland, Espoo, Finland (see <http://www.vtt.fi/>).

⁵ Advanced Interconnect Technology Limited, Hong Kong (see <http://www.ait.com.hk>).

⁶ See <http://www-ppd.fnal.gov/MTBF-w/>.