Real-Time Embedded System Support for the BTeV Level 1 Muon Trigger

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RTES Collaboration

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Real Time Embedded Systems Collaboration

- Funded by the National Science Foundation
  - Information Technology Research Program

- Consisting of:
  - University of Illinois
    - Center for Reliable and High-Performance Computing (CRHC) of the Coordinated Science Laboratory (CSL)
      - » Design and Validation of Reliable Networked Systems Research Group
      - » D. Beauregard, R. Iyer, Z. Kalbarczyk, Q. Liu, L. Wang
    - High Energy Physics Group of the Department of Physics
      - » M. Haney, M. Selen
  - University of Pittsburgh
    - Fault Tolerant Real-Time Systems (FORTS) Group in the Department of Computer Science
      - » D. Mosse, O. Shigiltchoff
    - Link-to-Learn educational program
    - College in High School educational program

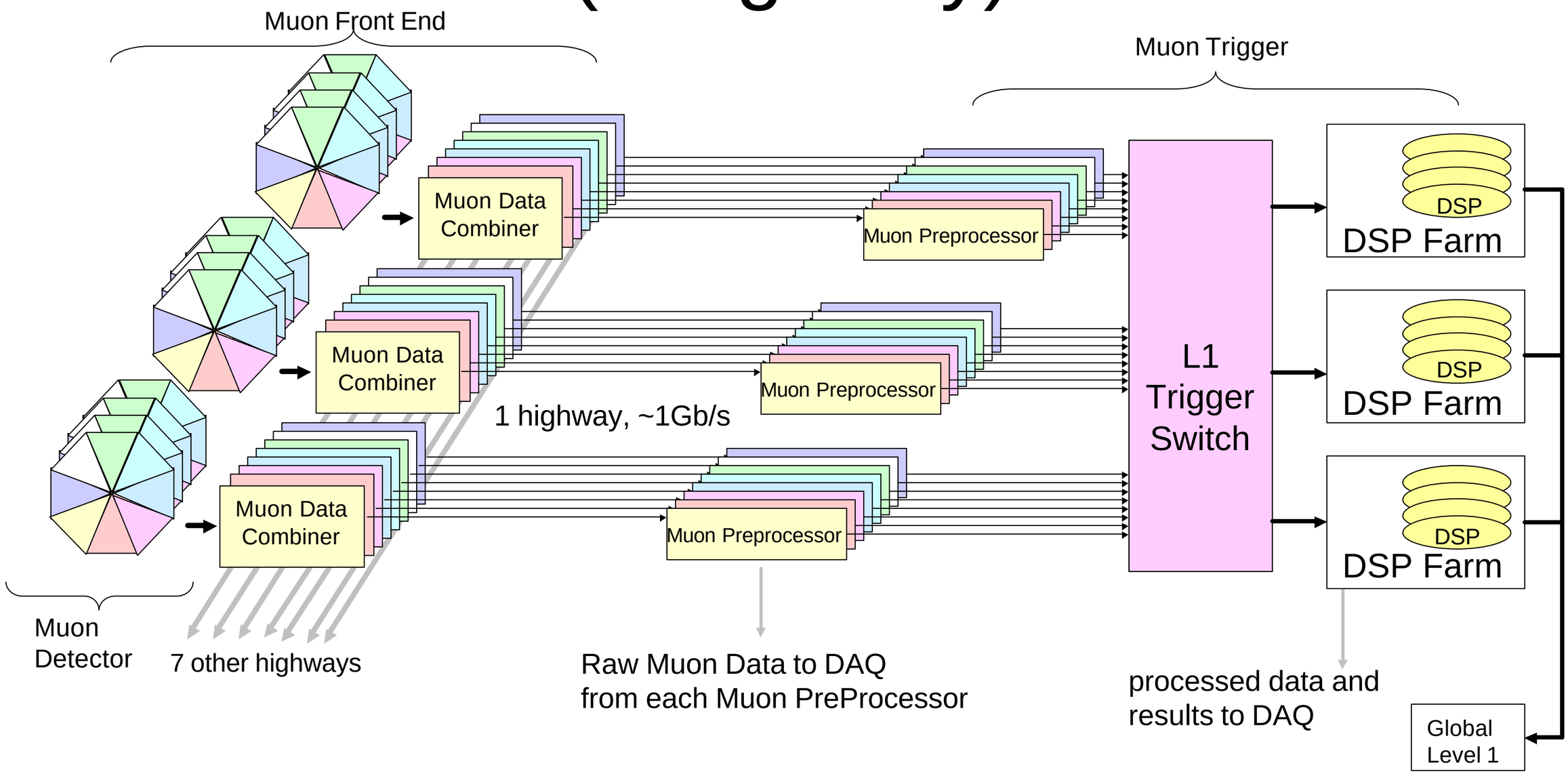
RTES Collaboration (2)

- Syracuse University
  - Department of Electrical Engineering and Computer Science
    - » R. Chopade, L. Hovey, M. Jung, D. Messie, J. Oh
  - High Energy Physics Group of the Department of Physics
    - » S. Stone
- Vanderbilt University
  - ISIS (Institute for Software Integrated Systems)
    - » T. Bapty, S. Neema, S. Nordstrom, S. Shetty, S. Vashishtha, D. Yao
  - BTeV Group, part of the High Energy Physics Group in the Department of Physics and Astronomy
    - » P. Sheldon, E. Vaandering
- Fermi National Accelerator Laboratory
  - BTeV Collaboration of the Particle Physics Division
    - » J. Butler, E. Gottschalk, J. Kowalkowski
  - Computing Division
    - » J. Kowalkowski, M. Votava
  - Fermilab Education Office
    - » J. Appel

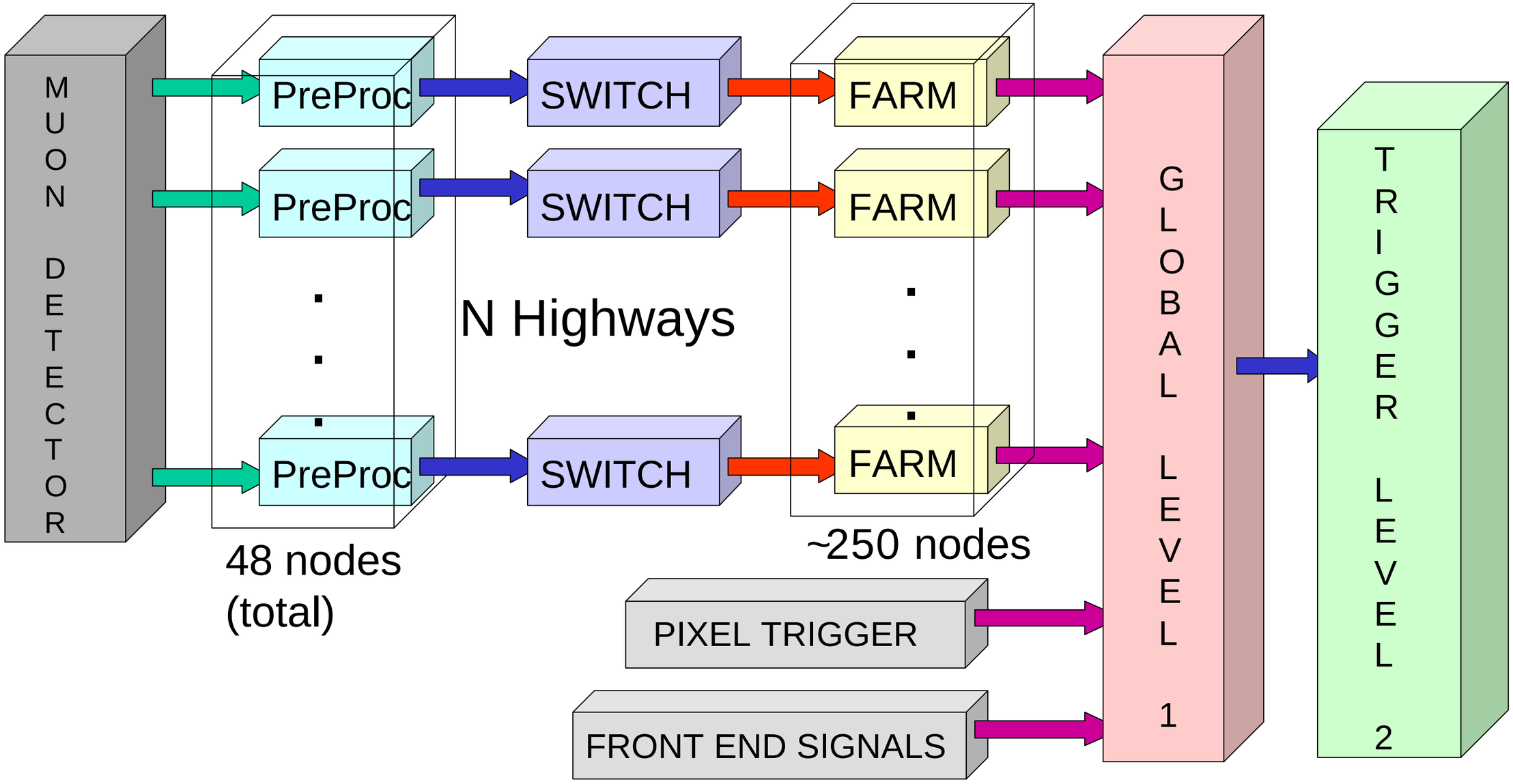
RTES Mission

- (from the NSF proposal)
  - to develop methodologies and tools for designing and implementing very large-scale real-time embedded computer systems that
    - achieve ultra high computational performance through use of parallel hardware architectures
    - achieve and maintain functional integrity via distributed, hierarchical monitoring and control
    - are required to be highly available
    - are dynamically reconfigurable, maintainable, and evolvable

BTeV L1 Muon Trigger Architecture (1 highway)



BTeV L1 Muon Trigger Architecture

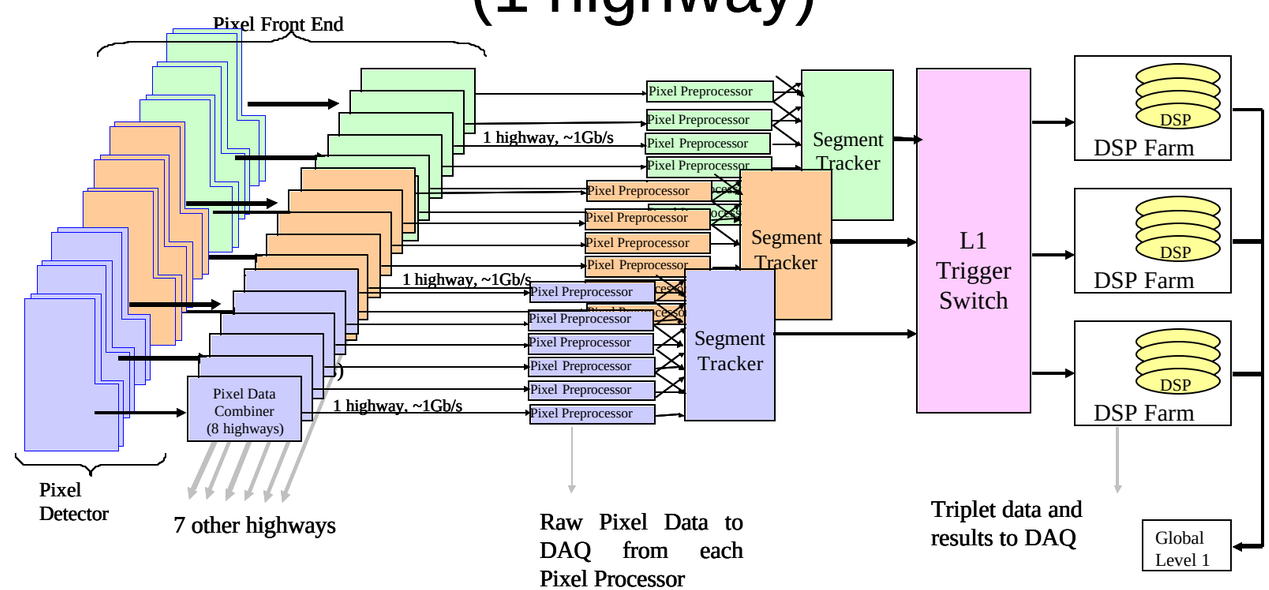


BTeV L1 Pixel Trigger

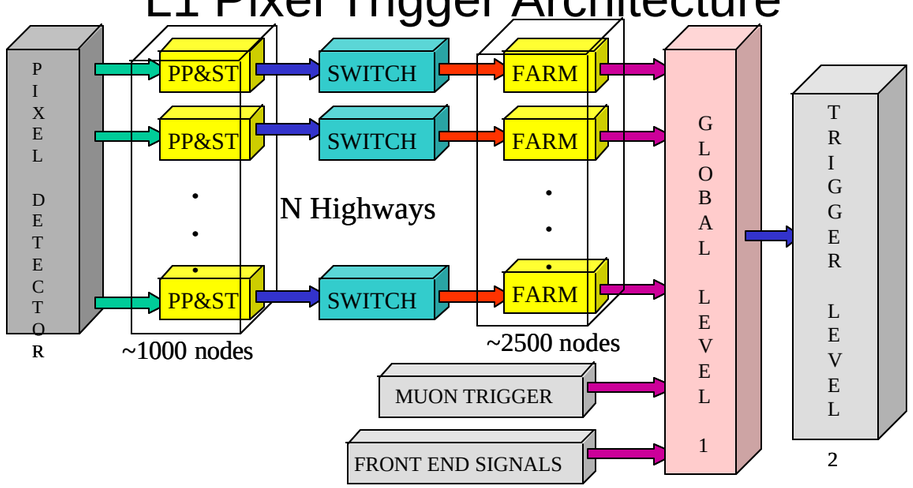
- It is no coincidence that the L1 Muon and Pixel Triggers are similar…

  (see also N29-7, N36-61)

L1 Pixel Trigger Architecture
(1 highway)



L1 Pixel Trigger Architecture



Shared architecture = design reuse
= substantial cost saving

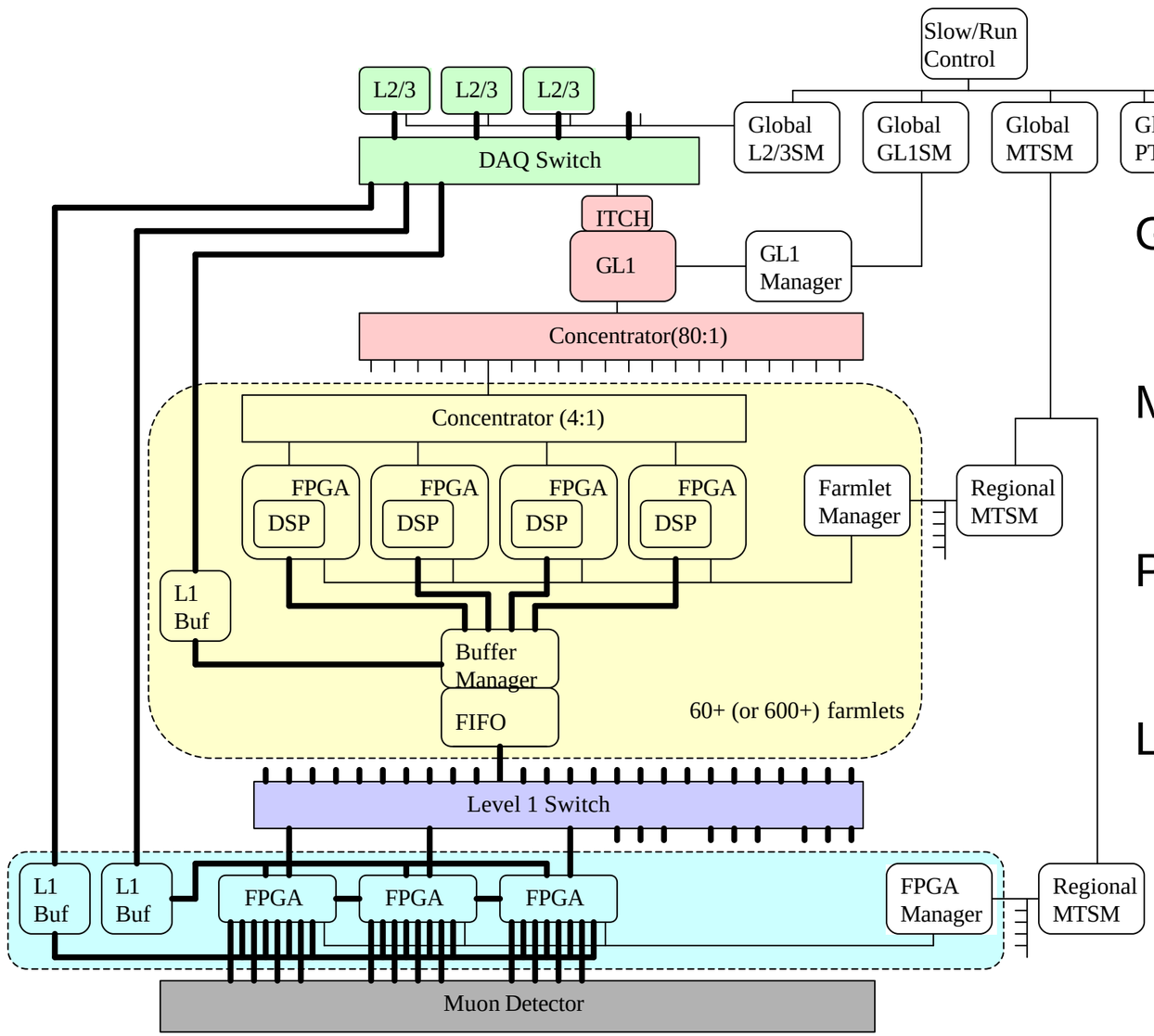
The Problem

- Large system
  - 100’s (1000’s) of FPGAs in the muon (pixel) trigger
  - 250+ (2500+) DSPs
  - 2500+ processor Linux farm
  - countless fiber cables, Cat-5 cables, backplanes…
- Something **will** fail !

- How do we get the best/most physics?
  - Detection, mitigation, graceful degradation

- RTES !

RTES view of the BTeV Trigger



GL1SM - Global L1 Trigger Supervisor/Monitor

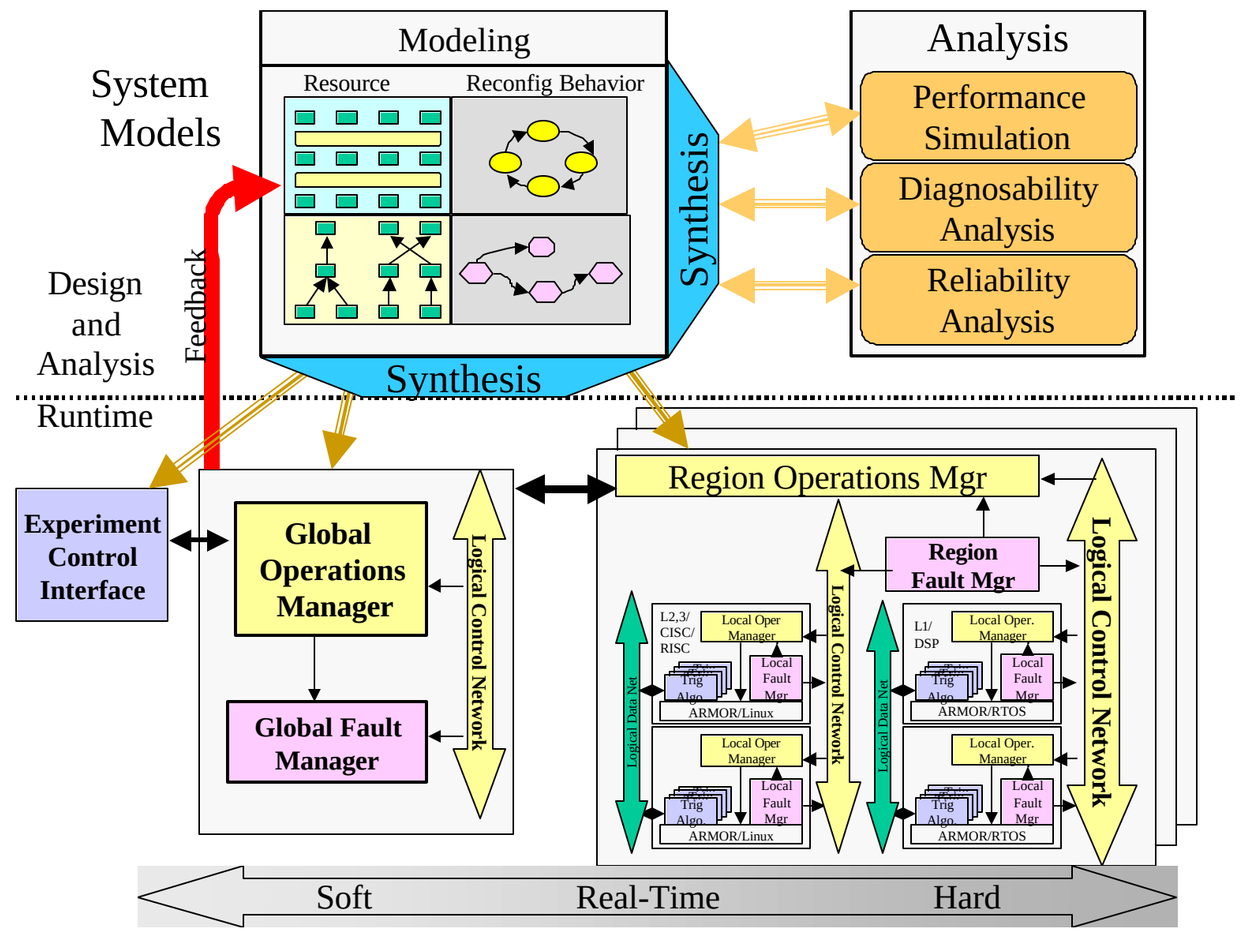
MTSM - Muon Trigger Supervisor/Monitor

PTSM - Pixel Trigger Supervisor/Monitor

L2/3SM - Level2/Level3 Trigger Supervisor/Monitor

RTES Solution

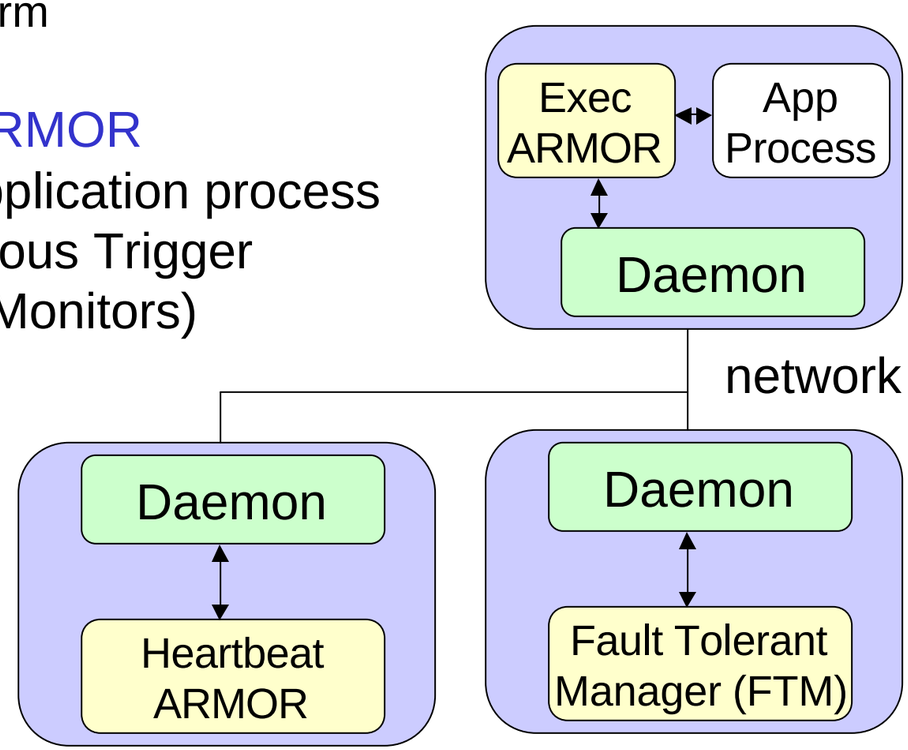
- Model Integrated Computing
  - Graphical representation of complex system, with modeling (simulation) resources
- ARMORs
  - To protect Linux processes
    - And subordinate DSP processes
- VLAs
  - To monitor/mitigate at every level
    - DSP, Supervisory Linux, Linux trigger farm, etc.



Adaptive Reconfigurable and Mobile Objects for Reliability

- On Linux/Windows machines…
  - Especially the xxSM supervisors and the L2/L3 farm

Execution ARMOR
Oversees application process (*e.g.* the various Trigger Supervisor/Monitors)

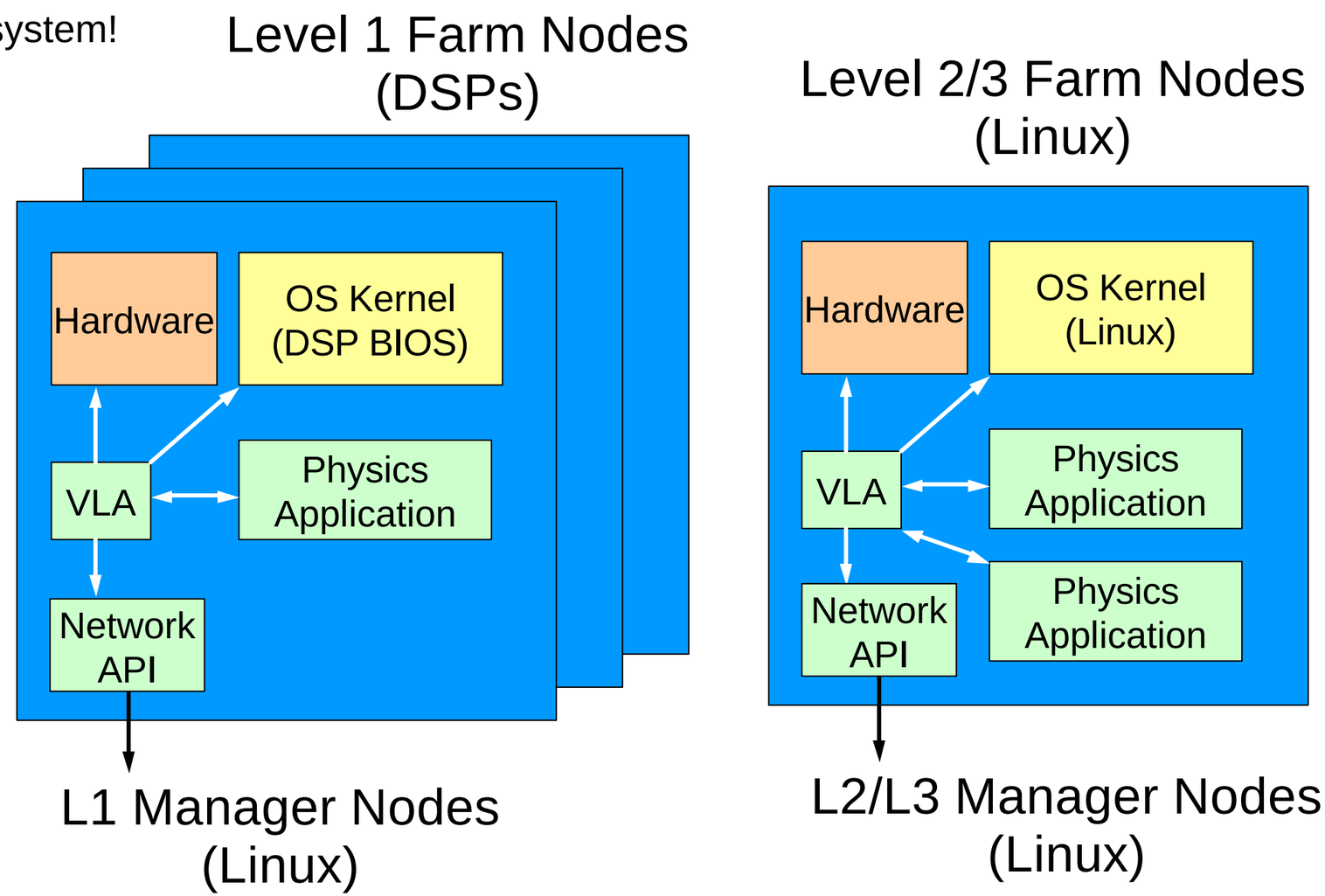


Daemons
Detect ARMOR crash and hang failures

Heartbeat ARMOR
Detects and recovers FTM failures

Fault Tolerant Manager
Highest ranking manager in the system

ARMOR processes
Provide a hierarchy of error detection and recovery. ARMORS are protected through checkpointing and internal self-checking.

Very Lightweight Agents

- Minimal footprint
- Platform independence
  - Employed everywhere in the system!
- Monitoring hardware and software
- Handles communications & control with higher level entities